



# DDR4 U-DIMM

Version 1.1 Jul. 19, 2021

**8GB U-DIMM**  
**DDR4-3200(CL22)**  
**AD4U320038G22-BHYD**

## General Description:

AD4U320038G22-BHYD is DDR4-3200(CL22)-22-22SDRAM memory module. The SPD is programmed to JEDEC standard latency 2666Mbps timing of 22-22-22at 1.2V. The module is composed of 8Gb CMOS DDR4 SDRAMs in FBGA package and one 4Kbit EEPROM in 8pin TDFN package on a 288pin glass-epoxy printed circuit board.

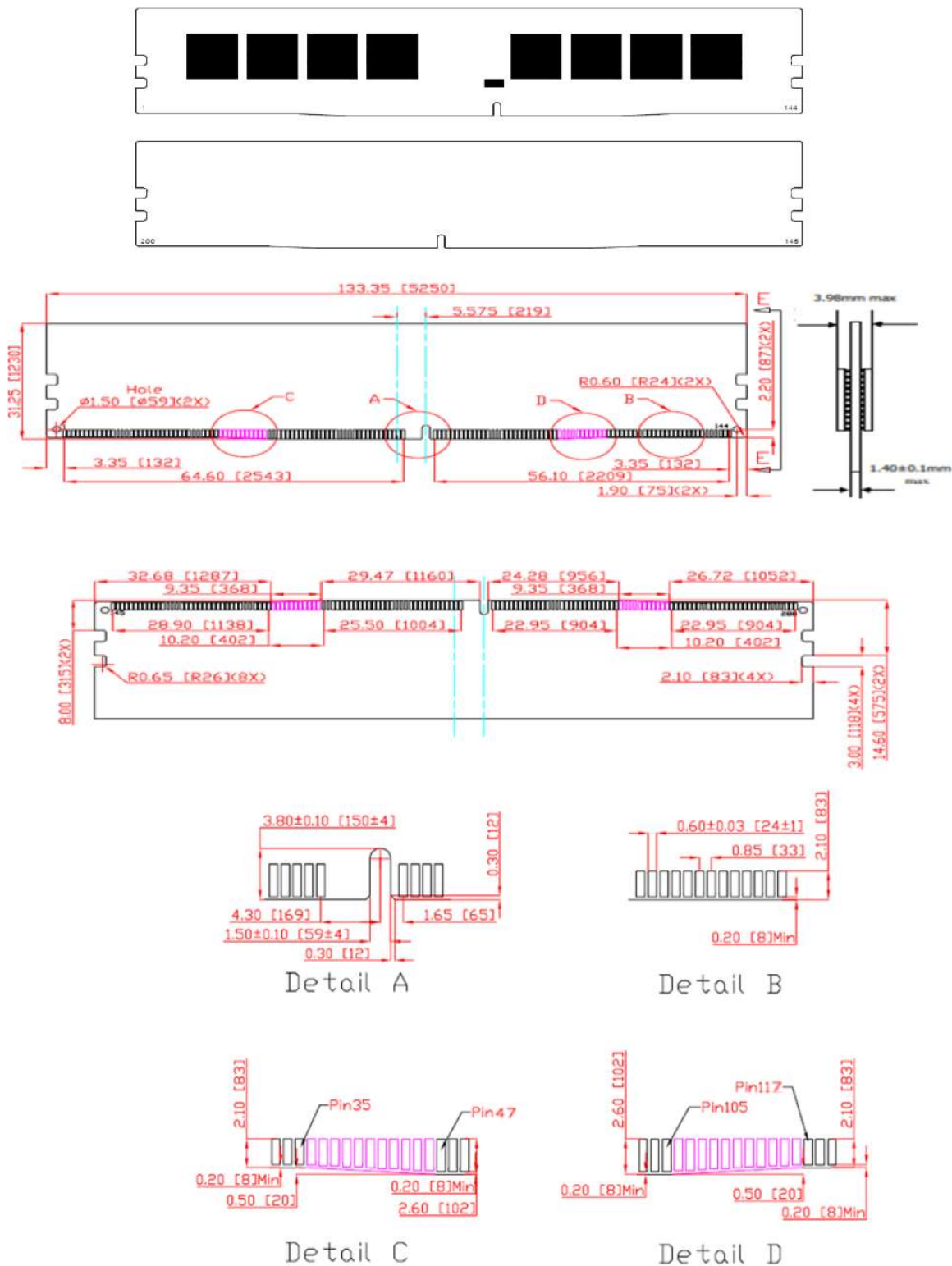
The module is a Dual In-line Memory Module and intended for mounting onto 288 pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

## Features:

- Power supply(Normal)
  - VDD & VDDQ = 1.2V +5% / -5%
  - VPP = 2.5V +10% / -5%
  - VDDSPD = 2.5V (2.25V to3.6V)
- Burst Length (BL):8 and 4 with Burst Chop(BC)
- Bi-directional, differential data strobe (DQS and /DQS)
- Differential clock input operation
- DLL aligns DQ and DQS transition with CK transition
- Double-data-rate architecture; two data transfers per clock cycle
- 16 internal banks; 4 groups of 4 banks each
- Internal self-calibration through ZQ pin (RZQ:240 ohm±1%)
- Low-power auto refresh(LPASR)
- Tc of 0°C to 95°C
  - 64ms, 8192-cycle refresh at 0°C to 85°C
  - 32ms, 8192-cycle refresh at 85°C to 95°C
- 8-bit pre-fetch architecture
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Data bus inversion for data bus(DBI)
- Data bus Write CRC
- Lead-free and Halogen-free products are RoHS Compliant

## Package Dimensions:

[8GB –1Rank, 1024Mx8DDR4SDRAMs]



Note: All dimensions are in millimeters(mils) and should be kept within a tolerance of  $\pm 0.15(5.91)$ , unless otherwise specified.



**Ordering Information:**



**Server /IPC DRAM Module P/N Decoder**

**AD 4 U 3200 3 8G 22 - B HY D**

**BRAND**

AD= ADATA

**Module MODE**

1= DDR                      4= DDR4  
2= DDR2  
3= DDR3  
D= DDR3L

**MODULE TYPE**

A=VLP SO-DIMM	M= Micro-DIMM
B= ECC SO-DIMM	R= R-DIMM
C= VLP ECC-DIMM	S= SO-DIMM
D= LR-DIMM	U= U-DIMM
E= ECC DIMM	V= VLP R-DIMM
F= FB-DIMM	X=VLP U-DIMM
I=SO-DIMM(W)	Y=VLP ECC
L=LR-DIMM 1.5H	SO-DIMM
H=ECC SO(W)	HR=R-DIMM(W)
HV=VLP R-DIMM(W)	HU= U-DIMM(W)

**SPEED**

1600= 1600MHz	1866= 1866MHz
2133= 2133MHz	2400= 2400MHz
2666= 2666MHz	2933= 2933MHz
3200= 3200MHz	

**COMPONENT CONFIG. CODE**

A= 64x8	H=32x8	6=4Gbx4
B= 128x8	I=128x4	<b>(DDP)</b>
C= 256x8	4=2048x4	J=512x16
D= 64x16	W=512x8	7=2048x8
E= 32x16	X=128x16	2=256x16
F= 256x4	Y=1024x4	8=1024x16
G= 512x4	3=1024x8	

**CAPACITY**

128M= 128M	4G= 4G
256M= 256M	8G= 8G
512M= 512M	16G=16G
1G= 1G	32G=32G
2G= 2G	64G=64G

**Die Version**

A=A Die	M =M Die
B=B Die	E = E Die
C=C Die	N = N Die
D=D Die	Q = Q Die
F =F Die	P = P Die
G=G Die	
H=H Die	
J =J Die	
K=K Die	
Z=Don't Care	

(IPC/Server)

**Die Source**

PF= PSC  
NA= NANYA  
HY=HYNIX  
PR=PROMOS  
EL=ELPIDA  
MI=MICRON  
SS=SAMSUNG  
AD=ADATA  
CX=CHANGXIN  
Z=Don't Care (IPC/Server)

**PACKAGE CODE**

B= Bulk  
R= Retail  
2= Dual-Kit Retail  
3= Tri-Kit Retail  
S= Single Tray  
RM= Retail MAC  
BUM= BULK+MAC HS

**CAS LATENCY**

2= CL2	7= CL7	15=CL15
25= CL2.5	8= CL8	17=CL17
3= CL3	9= CL9	19=CL19
4= CL4	10=CL10	22=CL22
5= CL5	11=CL11	
6= CL6	13=CL13	