Date	Revision	Item
2022/11/24	Ver 1.0	First Released

DDR5 SO DIMM

Specification

P/N :

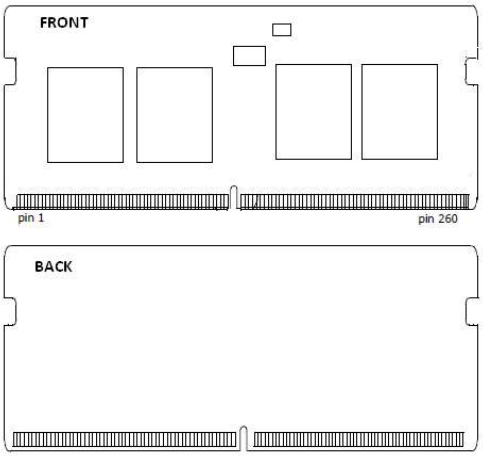
HSG4HK1-CE6UEC-KKAV
HSH2HK1-C28NEC-JKAV
HSI8HK1-C28NEC-MKAV

DDR5 SO-DIMM 1Gx64/2Gx64/4Gx64

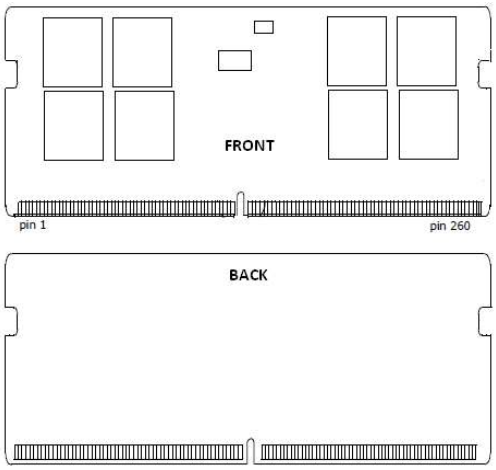
Features

- DRAM VDD/VDDQ = 1.1V (-33mV / +66mV)
- DRAM VPP = 2.5V (–125mV / +250mV)
- 32 Bank with x8
- 16 Bank with x16
- 8 BG(Bank Group) for X8/X16 configurations
- BL16, BC8 OTF, BL32, BL32 OTF supported
- Same Bank Refresh
- VrefDQ / VrefCA / VrefCS Training
- Hard/Soft Post Package Repair
- Input Clock Frequency Change
- Maximum Power Saving Mode (MPSM)
- Multi-Purpose Command (MPC)
- Per DRAM Addressability (PDA)
- Read Training Mode
- CA Training Mode
- CS Training Mode
- Per Pin VREFDQ Training
- Write Leveling Training Mode
- Connectivity Test (CT)
- ZQ Calibration
- DFE (Decision Feedback Equalization) for DQ
- DQS Interval Oscillator
- 1N / 2N Mode support for Commands
- On-Die ECC
- ECC Transparency and Error Scrub
- CRC (Cyclic Redundancy Check)
- Loopback for multiple purposes - monitor data, BER(Bit Error Rate) analysis, etc.
- Training Modes:
  - VrefDQ / VrefCA / VrefCS Training
  - Read Training Mode
  - CA Training Mode
  - CS Training Mode
  - Per Pin VREFDQ Training
  - Write Leveling Training Mode
  - Duty Cycle Adjuster (DCA) for Read - Global
  - Per Pin DCA(Duty Cycle Adjuster) for Read – Per Pin(DQ).
- Operating temperature:
  - Commercial (0°C ≤ TOPER ≤ +95°C)

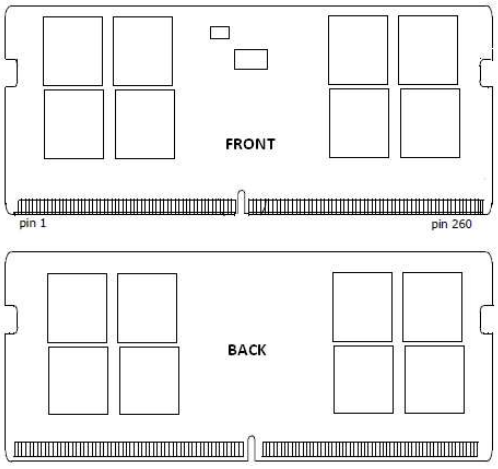
8GB by x16(1Rank)



16GB by x8(1Rank)



32GB byx8(2Rank)



Part No. Information

Part Number	Module Density	MT/s	Module Bandwidth	Module Organization	DRAM IC Composition	Ranks of Module
HSG4HK1-CE6UEC-KKAV	8GB	4800	38400GB/s	1Gx64	1Gbx16	1
HSH2HK1-C28NEC-JKAV	16GB	4800	38400GB/s	2Gx64	2Gbx8	1
HSI8HK1-C28NEC-MKAV	32GB	4800	38400GB/s	4Gx64	2Gbx8	2

Key Parameters

MT/s	tCK (ns)	CAS Latency(ns)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP (tCK)
DDR5-4800	0.416	16	16	16	32	48	40-40-40

Address Table

		8GB (1Rx16)	16GB (1Rx8)	32GB (2Rx8)
Bank Address	# of Bank Groups	4 / 4 / 16	8 / 4 / 32	8 / 4 / 32
	BG Address	BG0~BG1	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		R0~R15	R0~R15	R0~R15
Column Address		C0~C9	C0~C9	C0~C9
Page size		2KB	1KB	2KB

Pin Assignments

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VIN_BULK	2	HSA	131	CK0_A_t	132	CK1_A_t
3	VIN_BULK	4	HSCL	133	CK0_A_c	134	CK1_A_c
5	RFU	6	HSDA	135	VSS	136	VSS
7	PWR_GOOD	8	PWR_EN	137	CK0_B_t	138	CK1_B_t
9	VSS	10	VSS	139	CK0_B_c	140	CK1_B_C
11	DQ0_A	12	DQ1_A	141	VSS	142	VSS
13	VSS	14	VSS	143	RFU	144	CA12_B
15	DQ2_A	16	DQ3_A	145	CA11_B	146	CA10_B
17	VSS	18	VSS	147	VSS	148	VSS
19	DM0_A_n	20	DQS0_A_C	149	CA9_B	150	CA8_B
21	VSS	22	DQS0_A_t	151	CA7_B	152	CA6_B
23	DQ4_A	24	VSS	153	VSS	154	VSS
25	VSS	26	DQ5_A	155	CA5_B	156	CA4_B
27	DQ6_A	28	VSS	157	CA3_B	158	CA2_B
29	VSS	30	DQ7_A	159	VSS	160	VSS
31	DQ8_A	32	VSS	161	CS0_B_n	162	CA1_B
33	VSS	34	DQ09_A	163	RESET_n	164	CA0_B
35	DQ10_A	36	VSS	165	CS1_B_N	166	VSS
37	VSS	38	DQ11_A	167	VSS	168	CB0_B
39	DQS1_A_C	40	VSS	169	DQS4_B_c	170	VSS
41	DQS1_A_t	42	DM1_A_n	171	DQS4_B_T	172	CB1_B
43	VSS	44	VSS	173	VSS	174	VSS
45	DQ12_A	46	DQ13_A	175	CB3_B	176	CB2_B
47	VSS	48	VSS	177	VSS	178	VSS
49	DQ14_A	50	DQ15_A	179	DQ0_B	180	DQ1_B
51	VSS	52	VSS	181	VSS	182	VSS
53	DQ16_A	54	DQ17_A	183	DQ2_B	184	DQ3_B
55	VSS	56	VSS	185	VSS	186	VSS
57	DQ18_A	58	DQ19_A	187	DM0_B_n	188	DQS0_B_C
59	VSS	60	VSS	189	VSS	190	DQS0_B_t
61	DM2_A_n	62	DQS2_A_C	191	DQ4_B	192	VSS
63	VSS	64	DQS2_A_t	193	VSS	194	DQ5_B
65	DQ20_A	66	VSS	195	DQ6_B	196	VSS
67	VSS	68	DQ21_A	197	VSS	198	DQ7_B
69	DQ22_A	70	VSS	199	DQ8_B	200	VSS
71	VSS	72	DQ23_A	201	VSS	202	DQ9_B
73	DQ24_A	74	VSS	203	DQ10_B	204	VSS
75	VSS	76	DQ25_A	205	VSS	206	DQ11_B

Pin Assignments (Continued)

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
77	DQ26_A	78	VSS	207	DQS1_B_C	208	VSS
79	VSS	80	DQ27_A	209	DQS1_B_t	210	DM1_B_n
81	DQS3_A_C	82	VSS	211	VSS	212	VSS
83	DQS3_A_t	84	DM3_A_n	213	DQ12_B	214	DQ13_B
85	VSS	86	VSS	215	VSS	216	VSS
87	DQ28_A	88	DQ29_A	217	DQ14_B	218	DQ15_B
89	VSS	90	VSS	219	VSS	220	VSS
91	DQ30_A	92	DQ31_A	221	DQ16_B	222	DQ17_B
93	VSS	94	VSS	223	VSS	224	VSS
95	CB0_A	96	CB1_A	225	DQ18_B	226	DQ19_B
97	VSS	98	VSS	227	VSS	228	VSS
99	CB2_A	100	DQS4_A_c	229	DM2_B_n	230	DQS2_B_C
101	VSS	102	DQS4_A_t	231	VSS	232	DQS2_B_t
103	CB3_A	104	VSS	233	DQ20_B	234	VSS
105	VSS	106	CS0_A_n	235	VSS	236	DQ21_B
107	CA0_A	108	ALERT_n	237	DQ22_B	238	VSS
109	CA1_A	110	CS1_A_n	239	VSS	240	DQ23_B
111	VSS	112	VSS	241	DQ24_B	242	VSS
113	CA2_A	114	CA3_A	243	VSS	244	DQ25_B
115	CA4_A	116	CA5_A	245	DQ26_B	246	VSS
117	VSS	118	VSS	247	VSS	248	DQ27_B
119	CA6_A	120	CA7_A	249	DQS3_B_c	250	VSS
121	CA8_A	122	CA9_A	251	DQS3_B_t	252	DM3_B_n
123	VSS	124	VSS	253	VSS	254	VSS
125	CA10_A	126	CA11_A	255	DQ28_B	256	DQ29_B
KEY				257	VSS	258	VSS
127	CA12_A	128	RFU	259	DQ30_B	260	DQ31_B
129	VSS	130	VSS	261	VSS	262	VSS

Pin Descriptions:

The pin description table below is a comprehensive list of all possible pins for DDR5 UDIMM/SODIMM devices. All pins listed may not be supported on a specific module.

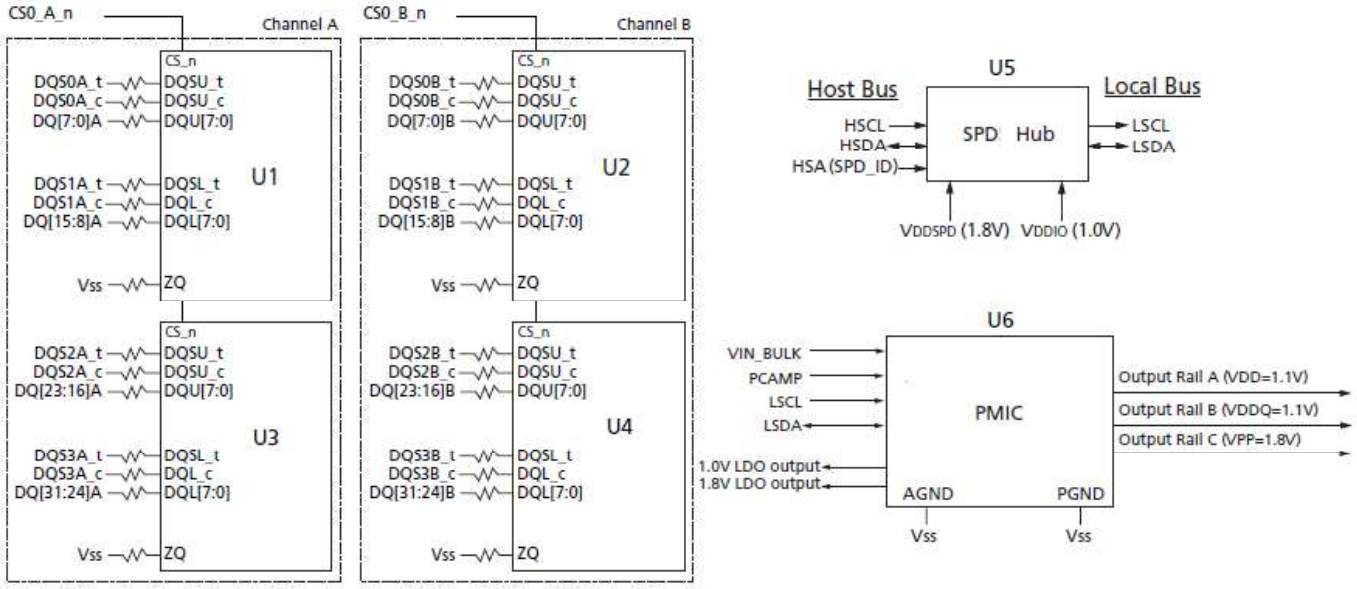
Pin Name	Type	I/O Level	Description
CA0_A ~ CA12_A CA0_B ~CA12_B	Input	VDDQ	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note that because some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during MODE REGISTER SET commands. The DDR5 component CA13 pin is strapped (connected) to eitherVSS or VDDQ depending on the strapped state of MIR.
CS0_A_n~ CS1_A_n CS0_B_n ~ CS1_B_n	Input	VDDQ	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down mode and self refresh mode. While not in self refresh mode the CS_n input buffer operates with the same ODT and VREF parameters as configured by the CA_ODT strap setting or mode register. When in self refresh, the CS_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDD.
DQ0_A ~ DQ31_A DQ0_B~DQ31_B	Input/ Output	VDDQ	Data Input/Output: Bidirectional data bus. If CRC is enabled via the mode register, THEN CRC CODE IS ADDED AT THE END OF DATA BURST. ANY DQ FROM DQ0–DQ3 may indicate the internal VREF level during test via mode register setting MR4 A4 =HIGH. Refer to the vendor-specific data sheets to determine which DQ is used.
CB0_A ~ CB3_A CB0_B ~CB3_B	Input/ Output	VDDQ	ECC Check Bits Input/Output: Bidirectional data bus. Only applicable on ECC SODIMM (SOEDIMM) or UDIMM (EUDIMM).
CK0_A_t, CK1_A_t CK0_B_t, CK1_B_t	Input	VDDQ	SDRAM Clocks CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CK0_A_c, CK1_A_c CK0_B_c, CK1_B_c			
DQS0_A_t~DQS4_A_t DQS0_B_t~DQS4_B_t	Input/ Output	VDDQ	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM only supports differential data strobe. It does not support single-ended strobe.
DQS0_A_c ~DQS4_A_c DQS0_B_c ~DQS4_B_c			
DM0_A_n ~DM3_A_n DM0_B_n~DM3_B_n	Input	VDDQ	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM function is shared with TDQS on x8 devices. The function of DM_n is enabled by MR5:OP[5] = 1. Refer to DDR5 component data sheet specification for further detail.
VIN_BULK	Supply		External Power Supply: 5V, 4.25V (min), 5.5V (max)

Pin Descriptions (Continued)

Pin Name	Type	I/O Level	Description
PWR_GOOD	Input Output	VDDQ	Power Good Indicator: Open drain output. The PMIC ensures this pin HIGH when VIN_Bulk input supply, as well as all enabled output buck regulators and all LDO regulators tolerance threshold is maintained as configured in the appropriate register. The PMIC drives this pin LOW when VIN_Bulk input goes below the threshold or when any of the enabled output buck regulator exceeds the thresholds configured in the appropriate register or when any LDO output regulator exceeds the threshold configured in the appropriate register. As an input, the PMIC disables its output regulator when this pin is LOW. The LDO outputs remain on.
HSCL	Input	VOUT_1.8V or VOUT_1.0V	Host Sideband Bus Clock: Bus clock used to strobe data into HUB device. When open drain, a pull-up resistor is required on the system motherboard.
HSDA	Input/ Output	VOUT_1.8V or VOUT_1.0V	Host Sideband Bus Data:I2C/I3C-Basic data. When open drain, a pull-up resistor is required on the system motherboard.
HSA	Input	GND	Host Sideband Bus Device ID: Address input to a hub or other client device to distinguish between identical devices in the I3C basic address range. Tied to GND,HSA has different resistor values on the motherboard to identify DIMM slot address. Refer to the SPD Hub spec for more information.
VSS	Supply		Ground
PWR_EN	Input		PMIC Enable: When this pin is HIGH, the PMIC turns on the regulator. When this pin is LOW, the PMIC turns off the regulator. This signal is connected to the PMIC's VR_EN pin.
RESET_n	CMOS Input	VDDQ	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDDQ.
ALERT_n	Output	VDDQ	Alert: If there is an error in CRC, then ALERT_n drives LOW for the period time interval and returns HIGH. During connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In the case where this pin is not connected, ALERT_n must be bonded to VDDQ on the system board.
RFU			Reserved for future use. No on DIMM electrical connection is present

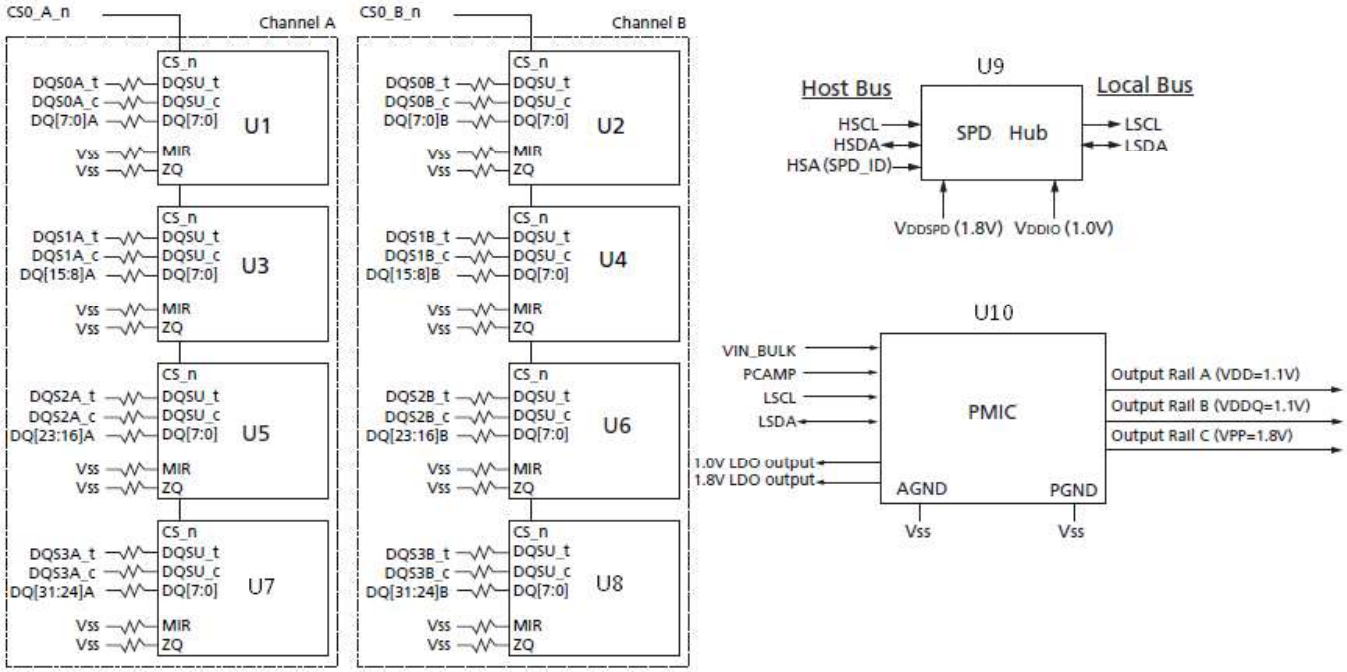
Functional Block Diagram:

8GB 1Gx64 (1Rank by x16)



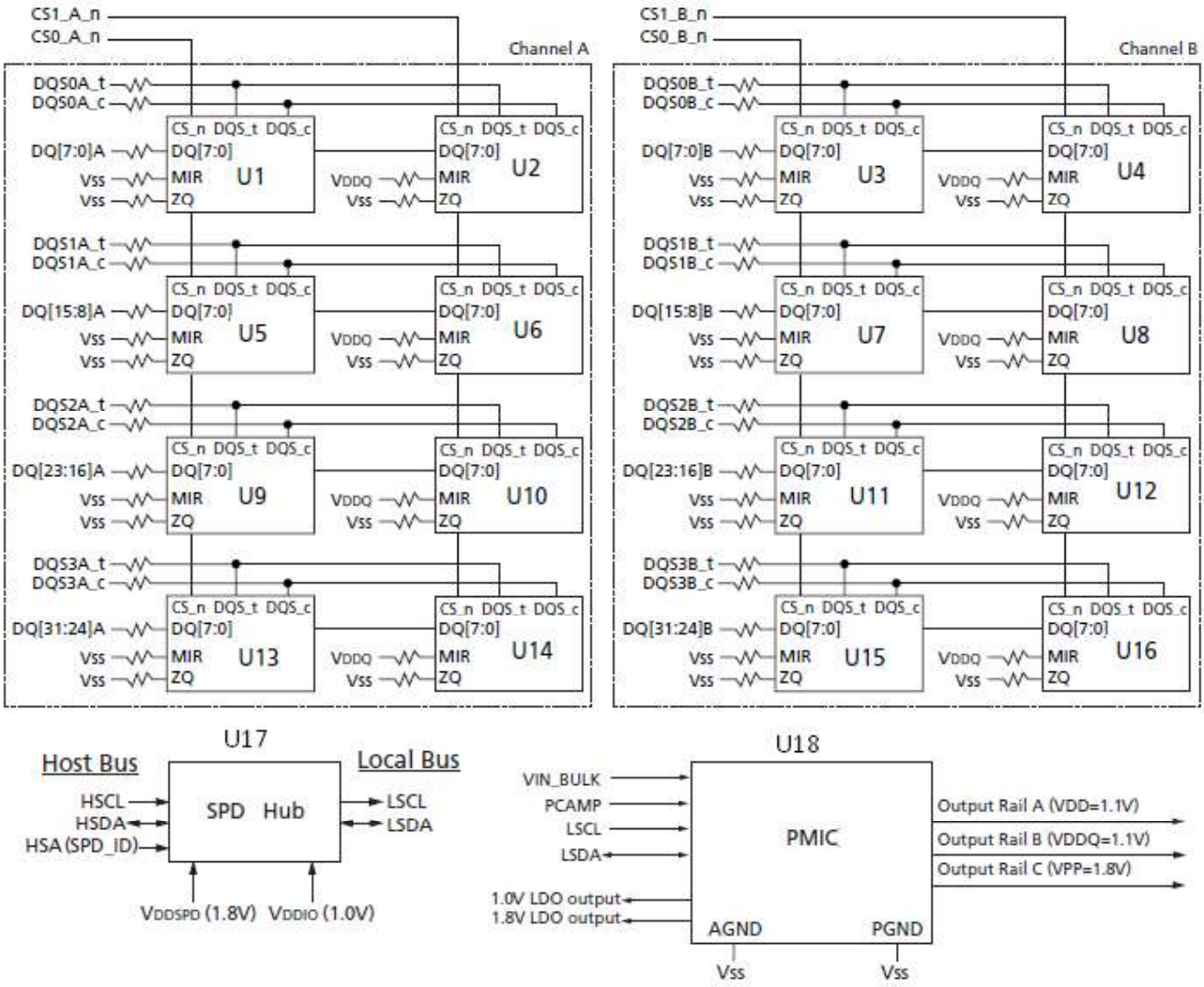
Note: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

16GB 2Gx64 (1Rank by x8)



Note: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

32GB 4Gx64 (2Rank by x8)



Note: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Electrical Specifications:

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	VDD supply voltage relative to VSS	-0.3 ~ 1.5	V	1,3
VDDQ	VDDQ supply voltage relative to VSS	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to VSS	-0.3 ~ 2.1	V	4
VIN, VOUT	Voltage on any pin relative to VSS	-0.3 ~ 1.5	V	1,3,5

Note:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times. When VDD and VDDQ are less than 500 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.
5. Overshoot area above 1.5 V is specified in Section 8.3.4, Section 8.3.5, and Section 8.3.6.

Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Device Supply Voltage	1.067(-3%)	1.1	1.166(+6%)	V
VDDQ	Supply Voltage for I/O	1.067(-3%)	1.1	1.166(+6%)	V
VPP	Core Power Voltage	1.746(-3%)	1.8	1.908(+6%)	V

Thermal Characteristics:

Symbol	Parameter/Condition	Value	Unit	Note
TC	Commercial operating case temperature	0 to 85	°C	1,2,3
TC		>85 to 95	°C	1,2,3,4
TOPER	Normal operating temperature range	0 to 85	°C	5
TOPER	Extended temperature operating range (optional)	>85 to 95	°C	5
TSTG	Non-operating storage temperature	–55 to 100	°C	6

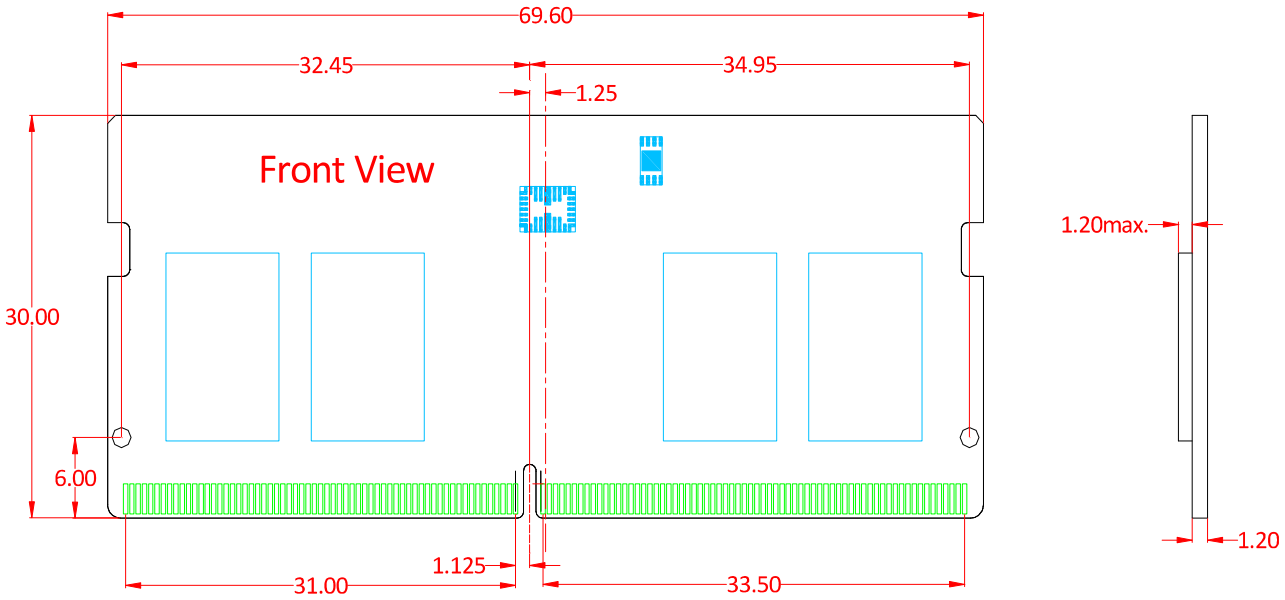
Notes:
1. Maximum operating case temperature; TC is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum TC during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum TC during operation.
4. If TC exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate.
5. The refresh rate must double when 85°C < TOPER ≤ 95°C.
6. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.

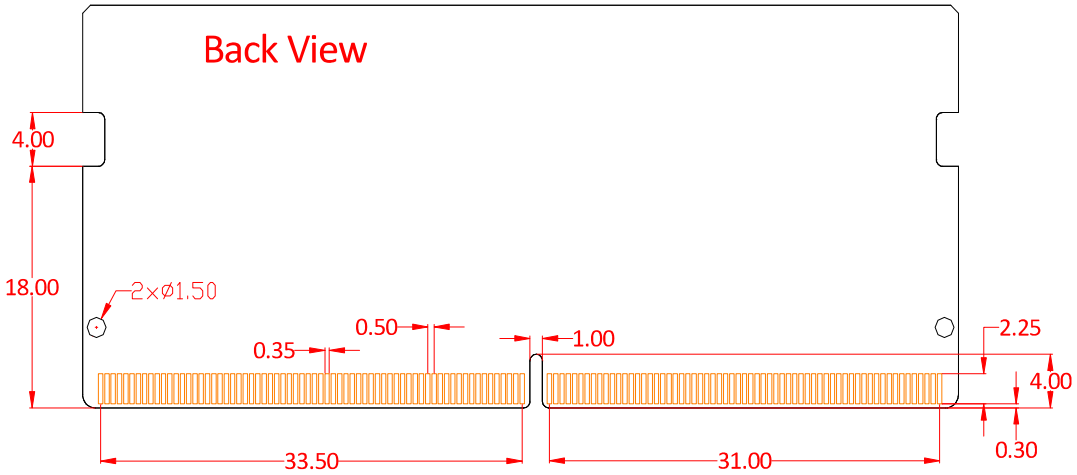
IDD Specifications:

Symbol	Parameter	8GB (1R byx16)	16GB (1R byx8)	32GB (2R byx8)	Unit
		4800	4800	4800	
IDD0	Operating one bank ACTIVATE-PRECHARGE current	98	127	247	mA
IDDF	Operating four bank ACTIVATE-PRECHARGE current	172	200	328	mA
IDD2N	Precharge standby current	74	98	219	mA
IDD2NT	Precharge standby non-target command	166	189	370	mA
IDD2P	Precharge power-down current	65	86	187	mA
IDD3N	Active standby current	81	116	249	mA
IDD3P	Active power-down current	75	104	221	mA
IDD4R	Operating burst read current	537	605	757	mA
IDD4W	Operating burst write current	778	844	993	mA
IDD4WC	Operating burst write with write CRC current	695	763	907	mA
IDD5B	Burst refresh (normal refresh mode) current	248	445	550	mA
IDD5F	Burst refresh (fine granularity refresh mode) current	160	270	373	mA
IDD5C	Burst refresh (same bank refresh mode) current	113	185	290	mA
IDD6N	Self refresh current	31	59	119	mA
IDD7	Operating bank interleave read current	634	684	825	mA
IDD8	Maximum power saving deep power down mode current	23	41	86	mA

Module Dimensions

8GB 1Gx64 (1Rank by x16)



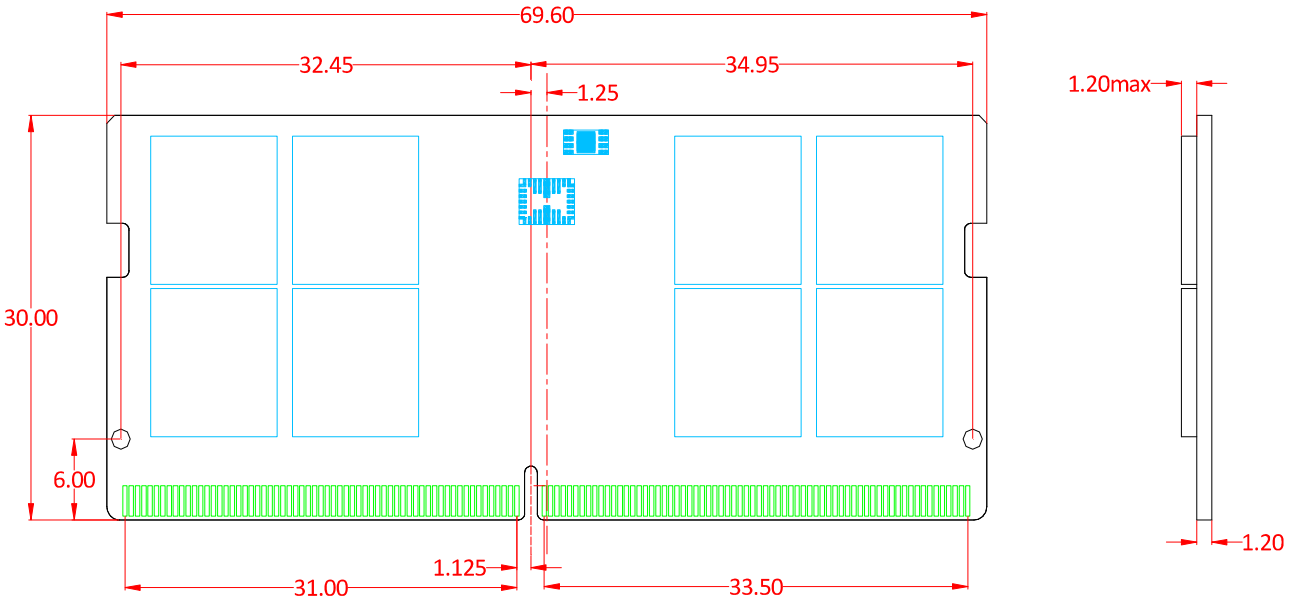


Notes:

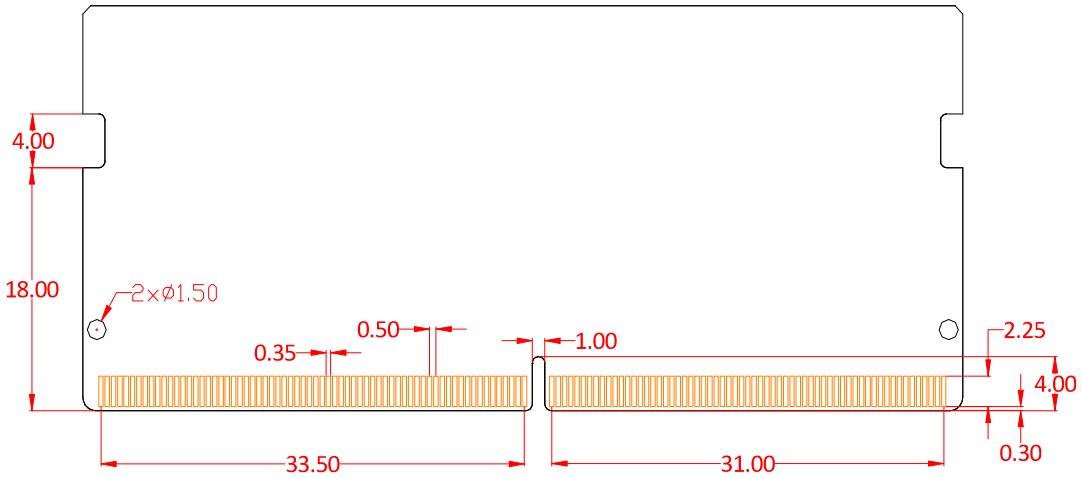
1. All dimensions are in millimeters.
2. Tolerance on all dimensions is ±0.15mm unless otherwise specified
3. The dimensional diagram is for reference only.

16GB 2Gx64 (1Rank by x8)

Front View

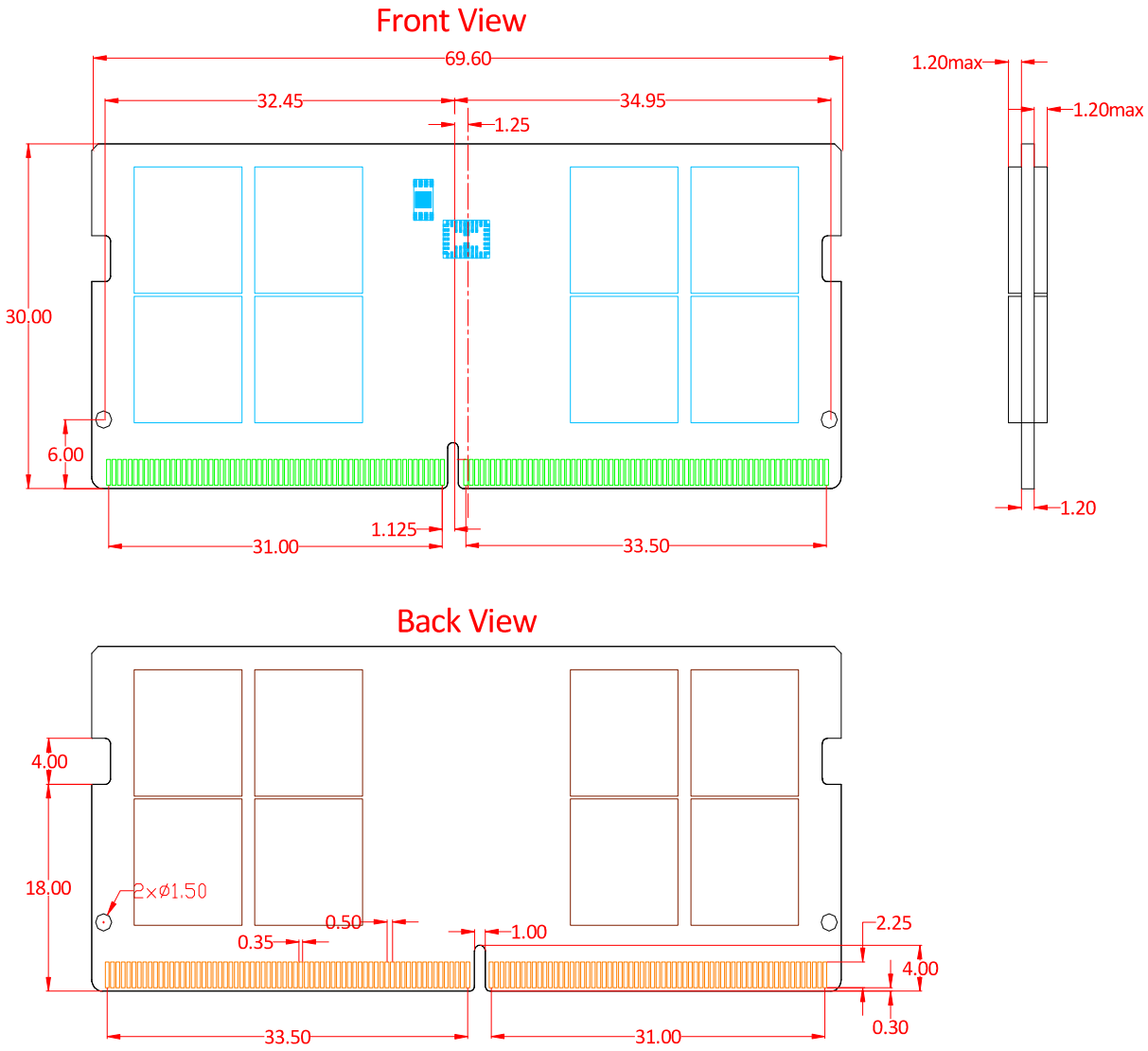


Back View



Notes: 1. All dimensions are in millimeters.
2. Tolerance on all dimensions is ±0.15mm unless otherwise specified
3. The dimensional diagram is for reference only.

32GB 4Gx64 (2Rank by x8)



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