ADATA®
INDUSTRIAL

DDR5 U-DIMM

(Photo for reference only.)

Version 1.0

Dec. 20, 2022

PC5-5600 | 1.1V | CL46

16GB

Revision History

Revision	Date	Description	Editor
1.0	Dec. 20, 2022	Initial release	Alan Peng

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1.0 General Description

AD5U560016G8-BHYA is DDR5-5600(CL46)-45-45 SDRAM memory module. The SPD is programmed to JEDEC standard latency 5600Mbps timing of 46-45-45 at 1.1V. The module is composed of 16Gb CMOS DDR5 SDRAMs in FBGA package and one 8Kbit SPD Hub in 8pin TDFN package on a 288pin glass–epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 288 pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

2.0 Key Features

- **Power supply (Normal)**
  - Vin_Bulk = 5V
  - VDD & VDDQ = 1.1V (+0.066V / -0.033V)
  - VPP = 1.8V (+0.108V / -0.054V)
  - VDDSPD = 1.8V (1.7V to 1.98V)
- **1.1V Pseudo open-drain I/O**
- **Burst Length (BL) 16 and 8 with Burst Chop(BC)**
- **Decision feedback equalization (DFE)**
- **32 internal banks; 8 groups of 4 banks each**
- **Tc of 0°C to 95°C**
  - 32ms,8192-cycle refresh at 0°C to 85°C
  - 16ms,8192-cycle refresh at 85°C to 95°C
- **All bank and same bank refresh**
- **Multi-purpose command (MPC)**
- **Loopback mode**
- **Data bus Write CRC**
- **CS/CA training mode**
- **On-die ECC**
- **ZQ Calibration**
- **1N/2N mode support for Commands**
- **Command-based non-target (NT) nominal, DQ/DQS park, and dynamic WR on-die termination(ODT)**
- **JEDEC Standard Compliant.**
- **Serial presence detect hub (SPD Hub) with Integrated temperature sensor**
- **Lead-free and Halogen-free products are RoHS Compliant.**

3.0 Pin Assignment and Descriptions

Table 3-1 Pin Assignment

288-Pin DDR5 UDIMM Front								288-Pin DDR5 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BULK	37	DQ20_A	73	CK0_A_c	109	V_{SS}	145	VIN_BULK	181	DQ22_A	217	CK1_A_c	253	V_{SS}
2	RFU	38	V_{SS}	74	V_{SS}	110	DQ5_B	146	VIN_BULK	182	V_{SS}	218	V_{SS}	254	DQ7_B
3	RFU	39	DQ21_A	75	RFU	111	V_{SS}	147	PWR_GOOD	183	DQ23_A	219	RFU	255	V_{SS}
4	HSCL	40	V_{SS}	76	RFU	112	DQ8_B	148	HSA	184	V_{SS}	220	RFU	256	DQ10_B
5	HSDA	41	DQ24_A	77	V_{SS}	113	V_{SS}	149	RFU	185	DQ26_A	221	V_{SS}	257	V_{SS}
6	V_{SS}	42	V_{SS}	78	CK0_B_t	114	DQ9_B	150	V_{SS}	186	V_{SS}	222	CK1_B_t	258	DQ11_B
7	RFU	43	DQ25_A	79	CK0_B_c	115	V_{SS}	151	PWR_EN	187	DQ27_A	223	CK1_B_c	259	V_{SS}
8	V_{SS}	44	V_{SS}	80	V_{SS}	116	DM1_B_n	152	RFU	188	V_{SS}	224	V_{SS}	260	DQS1_B_c
9	DQ0_A	45	DM3_A_n	81	RFU	117	V_{SS}	153	V_{SS}	189	DQS3_A_c	225	RFU	261	DQS1_B_t
10	V_{SS}	46	V_{SS}	82	CA12_B	118	DQ12_B	154	DQ2_A	190	DQS3_A_t	226	RFU	262	V_{SS}
11	DQ1_A	47	DQ28_A	83	V_{SS}	119	V_{SS}	155	V_{SS}	191	V_{SS}	227	V_{SS}	263	DQ14_B
12	V_{SS}	48	V_{SS}	84	CA10_B	120	DQ13_B	156	DQ3_A	192	DQ30_A	228	CA11_B	264	V_{SS}
13	DQS0_A_c	49	DQ29_A	85	CA8_B	121	V_{SS}	157	V_{SS}	193	V_{SS}	229	CA9_B	265	DQ15_B
14	DQS0_A_t	50	V_{SS}	86	V_{SS}	122	DQ16_B	158	DM0_A_n	194	DQ31_A	230	V_{SS}	266	V_{SS}
15	V_{SS}	51	CB0_A	87	CA6_B	123	V_{SS}	159	V_{SS}	195	V_{SS}	231	CA7_B	267	DQ18_B
16	DQ4_A	52	V_{SS}	88	CA4_B	124	DQ17_B	160	DQ6_A	196	CB2_A	232	CA5_B	268	V_{SS}
17	V_{SS}	53	CB1_A	89	V_{SS}	125	V_{SS}	161	V_{SS}	197	V_{SS}	233	V_{SS}	269	DQ19_B
18	DQ5_A	54	V_{SS}	90	CA2_B	126	DQS2_B_c	162	DQ7_A	198	CB3_A	234	CA3_B	270	V_{SS}
19	V_{SS}	55	DQS4_A_c	91	CA0_B	127	DQS2_B_t	163	V_{SS}	199	V_{SS}	235	CA1_B	271	DM2_B_n
20	DQ8_A	56	DQS4_A_t	92	V_{SS}	128	V_{SS}	164	DQ10_A	200	ALERT_n	236	V_{SS}	272	V_{SS}
21	V_{SS}	57	V_{SS}	93	CS0_B_n	129	DQ20_B	165	V_{SS}	201	V_{SS}	237	CS1_B_n	273	DQ22_B
22	DQ9_A	58	CS0_A_n	94	V_{SS}	130	V_{SS}	166	DQ11_A	202	CS1_A_n	238	V_{SS}	274	V_{SS}
23	V_{SS}	59	V_{SS}	95	RESET_n	131	DQ21_B	167	V_{SS}	203	V_{SS}	239	DQS4_B_c	275	DQ23_B
24	DM1_A_n	60	CA0_A	96	V_{SS}	132	V_{SS}	168	DQS1_A_c	204	CA1_A	240	DQS4_B_t	276	V_{SS}
25	V_{SS}	61	CA2_A	97	CB0_B	133	DQ24_B	169	DQS1_A_t	205	CA3_A	241	V_{SS}	277	DQ26_B
26	DQ12_A	62	V_{SS}	98	V_{SS}	134	V_{SS}	170	V_{SS}	206	V_{SS}	242	CB2_B	278	V_{SS}
27	V_{SS}	63	CA4_A	99	CB1_B	135	DQ25_B	171	DQ14_A	207	CA5_A	243	V_{SS}	279	DQ27_B
28	DQ13_A	64	CA6_A	100	V_{SS}	136	V_{SS}	172	V_{SS}	208	CA7_A	244	CB3_B	280	V_{SS}
29	V_{SS}	65	V_{SS}	101	DQ0_B	137	DM3_B_n	173	DQ15_A	209	V_{SS}	245	V_{SS}	281	DQS3_B_c
30	DQ16_A	66	CA8_A	102	V_{SS}	138	V_{SS}	174	V_{SS}	210	CA9_A	246	DQ2_B	282	DQS3_B_t
31	V_{SS}	67	CA10_A	103	DQ1_B	139	DQ28_B	175	DQ18_A	211	CA11_A	247	V_{SS}	283	V_{SS}
32	DQ17_A	68	V_{SS}	104	V_{SS}	140	V_{SS}	176	V_{SS}	212	V_{SS}	248	DQ3_B	284	DQ30_B
33	V_{SS}	69	CA12_A	105	DQS0_B_c	141	DQ29_B	177	DQ19_A	213	RFU	249	V_{SS}	285	V_{SS}
34	DQS2_A_c	70	RFU	106	DQS0_B_t	142	V_{SS}	178	V_{SS}	214	RFU	250	DM0_B_n	286	DQ31_B
35	DQS2_A_t	71	V_{SS}	107	V_{SS}	143	RFU	179	DM2_A_n	215	V_{SS}	251	V_{SS}	287	V_{SS}
36	V_{SS}	72	CK0_A_t	108	DQ4_B	144	RFU	180	V_{SS}	216	CK1_A_t	252	DQ6_B	288	RFU

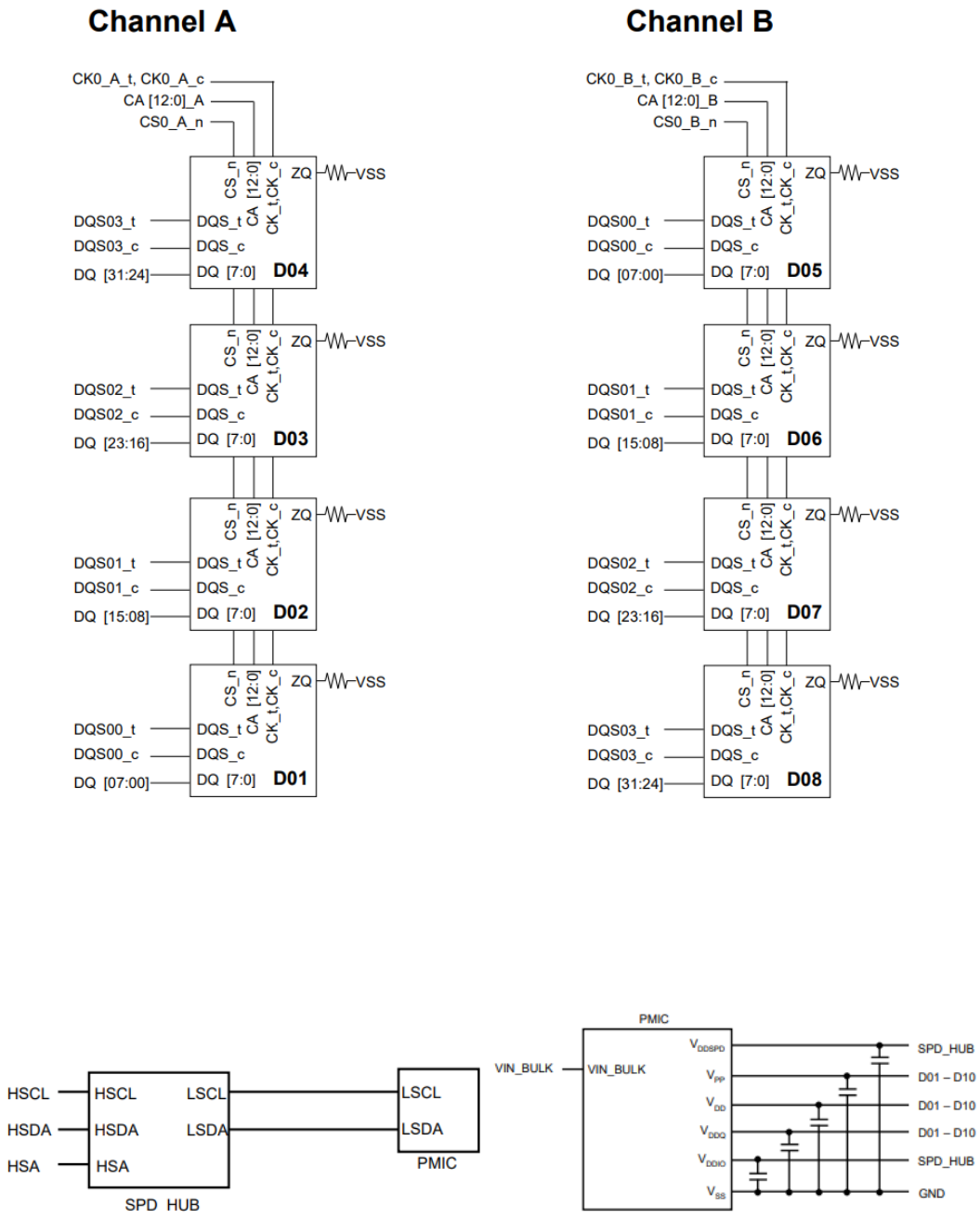
Table 3-2 Pin Descriptions

Pin Name	Description	Pin Name	Description
CA[12:0]_A CA[12:0]_B	Address and Command Bus	DQ[31:0]_A DQ[31:0]_B	DIMM memory Data bus channel A & B
CS[1:0]_A CS[1:0]_B	Chip Select	CB[7:0]_A CB[7:0]_B	DIMM ECC Checkbits (CB) channel A & B
PAR_A PAR_B	Parity input	DQS[9:0]_A_t DQS[9:0]_B_t	Data Strobes (positive line of differential pair)
CK_t	Clocks (true/positive)	DQS[9:0]_A_c DQS[9:0]_B_c	Data Strobes (negative line of differential pair)
CK_c	Clocks (complement/negative)	TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.
ALERT_n	Alert for CRC error	TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.
RESET_n	Set DRAM to known state	VIN_BULK	DIMM Power Supply from system to PMIC
PCAMP	Control and Monitor Port	VIN_MGMT	DIMM Power Supply from system to PMIC
HSCL	I2C/I3C-Basic Host Sideband Bus Clock	VSS	Power supply return (ground)
HSDA	I2C/I3C-Basic Host Sideband Bus Data	RFU	Reserved for future use
HSA	I2C/I3C-Basic Host Sideband Bus Address	LBDQS	Loopback Data strobe output
LBDQ	Loopback Data output:		

1. TDQSx and DQSx_t share a pin..
2. DDR5 UDIMM has 2 channels (channel-A and channel-B) of signal bus. The signals with suffix: _A (e.g. DQ0_A) are for channel-A, and the signals with suffix: _B (e.g. DQ0_B) are for channel-B

4.0 Function Block Diagram

Figure 4-1 1Rank, x8 DDR5 SDRAMs



Note : ZQ resistors are 240 Ω ± 1%.

5.0 Absolute Maximum Ratings

Table 5-1 Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit
Voltage on VDD supply relative to Vss	VDD	-0.3 ~ 1.4	V
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.4	V
Voltage on VPP pin relative to Vss	VPP	-0.3 ~ 2.1	V
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.4	V
Storage temperature	TSTG	-55 ~ +100	℃

Notes:

DDR5 SDRAM component specification.

6.0 Operation Temperature Condition

Table 6-1 Operation Temperature Condition

Parameter	Symbol	Value	Unit	Note
Normal Operating Temperature Range	TC	0~+85	℃	
Extended Temperature Range (Optional)	TC	+85~+95	℃	1

Notes:

(1) Refresh commands must be doubled in frequency, reducing the refresh interval tREFI to 1.95 μs

7.0 DC Operating Condition

Voltage referenced to Vss=0V,VDD&VDDQ=1.1V(+0.066V/-0.033V),Tc = 0 to 85 ℃

Table 7-1 DC Operating Condition

Parameter	Symbol	Min.	Typ.	Max	Unit	Note
Host Supply Voltage	VIN_BULK	4.25	5.0	5.5	V	
PMIC Output Supply Voltage	VDD	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VDDQ	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VPP	1.746	1.8	1,908	V	3
PMIC Output Supply Voltage	VDDSPD	1.70	1.8	1.98	V	

Notes:

(1) VDD must be within 66mv of VDDQ

(2) AC parameters are measured with VDD and VDDQ tied together.

(3) This includes all voltage noise from DC to 2 MHz at the DRAM package ball.

8.0 AC & DC Input Measurement Levels

Overshoot and Undershoot specifications for CAC - No Ballot

9.0 IDD Specification

Table 9-1 VDDQ = VDD = 1.1V(1.067V~1.166V),PC5-5600

Symbol	Condition	16GB	Unit
IDD0	One bank ACTIVATE-PRECHARGE current	TBD	mA
IDD0F	Operating Four Bank Active-Precharge Current	TBD	mA
IDD2N	Precharge Standby Current	TBD	mA
IDD2P	Precharge Power-Down Current	TBD	mA
IDD3N	Active standby current	TBD	mA
IDD3P	Active Power-Down Current	TBD	mA
IDD4R	Burst Read Current	TBD	mA
IDD4W	Burst write current	TBD	mA
IDD5B	Burst Refresh Current (1x REF)	TBD	mA
IDD5C	Burst Refresh Current (Same Bank Refresh Mode)	TBD	mA
IDD6N	Self refresh current: Normal temperature range (0–85°C)	TBD	mA
IDD7	Bank interleave read current	TBD	mA
IDD8	Maximum power-down current	TBD	mA

10.0 Timings used for IDD, IPP and IDDQ Measurement

Table 10-1 Timings used for IDD, IPP and IDDQ Measurement

Symbol	DDR5-4400	DDR5-4800	DDR5-5200	DDR5-5600	DDR5-6000	DDR5-6400	Units
Bin(CL-tRCD-tRP)	36-36-36	40-39-39	42-42-42	46-45-45	48-48-48	52-52-52	
Parameter	Min	Min	Min	Min	Min	Min	
tCK	0.454	0.416	0.385	0.357	0.333	0.312	ns
CL	36	40	42	46	48	52	nCK
CWL	36	39	42	45	48	52	nCK
nRCD	36	49	42	45	48	52	nCK
nRC	70	77	83	89	96	102	nCK
nRAS	106	115	125	134	144	153	nCK
nRP	36	39	42	45	48	52	nCK
nRFC 8Gb	430	469	506	546	586	625	nCK
nRFC 16Gb	650	709	766	826	886	946	nCK
nRFC 32Gb	TBD	TBD	TBD	TBD	TBD	TBD	nCK

11.0 Timing Parameters

Table 11-1 Timing Parameters

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock Timing									
Clock period average	tCK (AVG)	0.416	<0.454	0.357	<0.384	0.312	<0.333	ns	1
Command and Address Timing									
Read to Read command delay for same bank group	tCCD_L	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	8
Write to Write command delay for same bank groupp	tCCD_L_WR	max(32nCK, 20ns)	–	max(32nCK, 20ns)	–	max(32nCK, 20ns)	–	nCK,ns	8
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	max(16nCK, 10ns)	–	max(16nCK, 10ns)	–	max(16nCK, 10ns)	–	nCK,ns	8
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6,8
Write to Read command delay for same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4,6,8
Read to Read command delay for different bank group	tCCD_S	8	–	8	–	8	–	nCK	8
Write to Write command delay for different bank group	tCCD_S_WR	8	–	8	–	8	–	nCK	8
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6,8
Write to Read command delay for different bank group	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4,6,8
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP						nCK,ns	2,4,6,8

Parameter	Symbol	DDR5-4800		DDR5-5600		DDR5-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	8
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	8
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8	–	8	–	8	–	nCK	8
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8	–	8	–	8	–	nCK	8
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 13.333ns)	–	Max(32nCK, 11.428ns)	–	Max(32nCK, 10.000ns)	–	nCK,ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 16.666ns)	–	Max(40nCK, 14.285ns)	–	Max(40nCK, 12.500ns)	–	nCK,ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	–	Max(12nCK, 7.5ns)	–	Max(12nCK, 7.5ns)	–	nCK,ns	8
Precharge to Precharge command delay	tPPD	2	–	2	–	2	–	nCK	7,8
Write recovery time	tWR	30	–	30	–	30	–	ns	8

Notes:

1. tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.
2. tCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + tWR(min) - tRTP(min), and when using the appropriate rounding algorithms,

   nCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + nWR(min) - nRTP(min).
3. RBL: Read burst length associated with Read command

   RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode

   RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode

   RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

4. WBL: Write burst length associated with Write command

   WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode

   WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode

   WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

5. 5 - The following is considered for tRTW equation

   1tCK needs to be added due to tDQS2CK

   Read DQS offset timing can pull in the tRTW timing

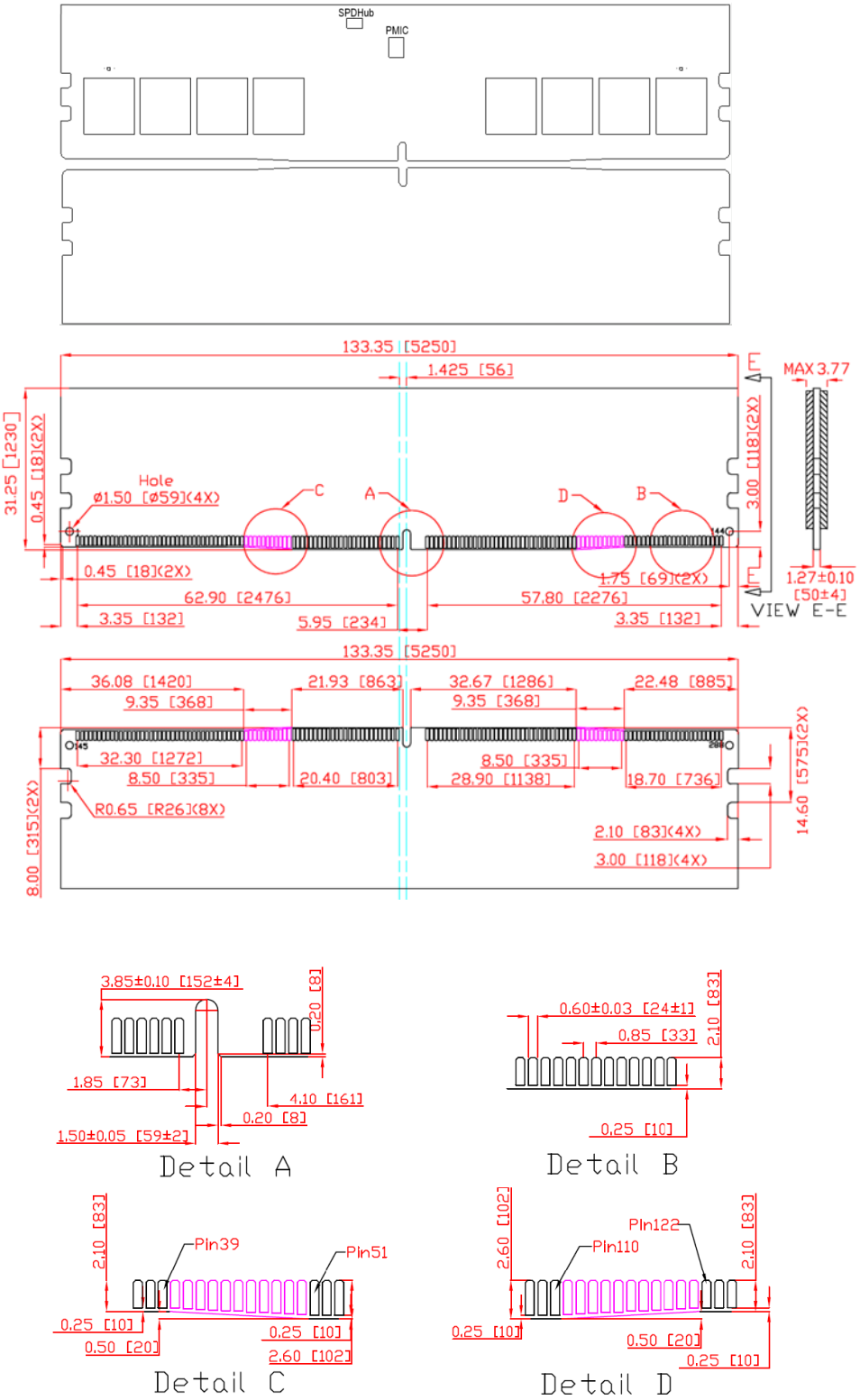
   1tCK needs to be added when 1.5tCK postamble

6. CWL=CL-2

7. tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a 3DS DDR5 SDRAM.

12.0 Physical Dimensions

Figure 12-1 Physical Dimensions



Notes:

All dimensions are in millimeters (mils) and should be kept within a tolerance of ± 0.15(5.91), unless otherwise specified.

13.0 Ordering Information

Figure 13-1 Ordering Information