Date	Revision	Item
2023/12/20	Ver 1.0	First Released

DDR5 UDIMM

Specification

P/N :

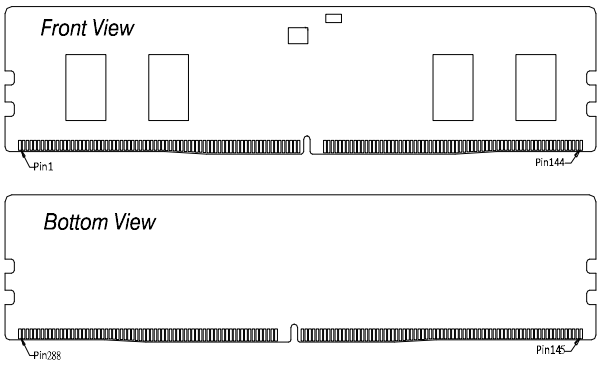
HLG4HK1-CE6UEC-EKAV
HLH2HK1-C28NEC-AKAV
HLI8HK1-C28NEC-CKAV
HLG4MN1-CE6UEC-EKAV
HLH2MN1-C28NEC-AKAV
HLH2MN1-C28IEC-AKAV
HLI8MN1-C28NEC-CKAV
HLI8MN1-C28IEC-CKAV

DDR5 UDIMM 1Gx64/2Gx64/4Gx64

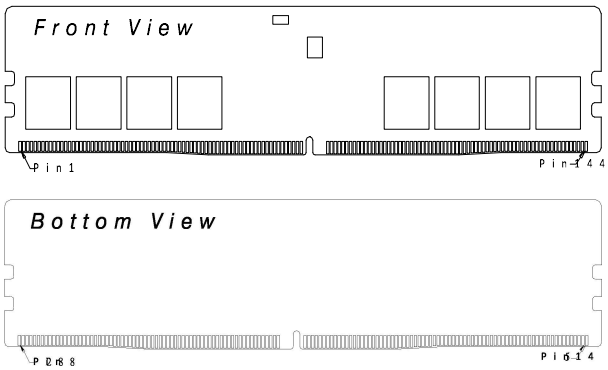
Features

- DRAM VDD/VDDQ = 1.1V (-33mV / +66mV)
- DRAM VPP = 2.5V (–125mV / +250mV)
- 32 Bank with x8
- 16 Bank with x16
- 8 BG(Bank Group) for X8/X16 configurations
- BL16, BC8 OTF, BL32, BL32 OTF supported
- Same Bank Refresh
- VrefDQ / VrefCA / VrefCS Training
- Hard/Soft Post Package Repair
- Input Clock Frequency Change
- Maximum Power Saving Mode (MPSM)
- Multi-Purpose Command (MPC)
- Per DRAM Addressability (PDA)
- Read Training Mode
- CA Training Mode
- CS Training Mode
- Per Pin VREFDQ Training
- Write Leveling Training Mode
- Connectivity Test (CT)
- ZQ Calibration
- DFE (Decision Feedback Equalization) for DQ
- DQS Interval Oscillator
- 1N / 2N Mode support for Commands
- On-Die ECC
- ECC Transparency and Error Scrub
- CRC (Cyclic Redundancy Check)
- Loopback for multiple purposes - monitor data, BER(Bit Error Rate) analysis, etc.
- Training Modes:
  - VrefDQ / VrefCA / VrefCS Training
  - Read Training Mode
  - CA Training Mode
  - CS Training Mode
  - Per Pin VREFDQ Training
  - Write Leveling Training Mode
  - Duty Cycle Adjuster (DCA) for Read - Global
  - Per Pin DCA(Duty Cycle Adjuster) for Read – Per Pin(DQ).
- Operating temperature:
  - Commercial (0°C ≤ TOPER ≤ +95°C)

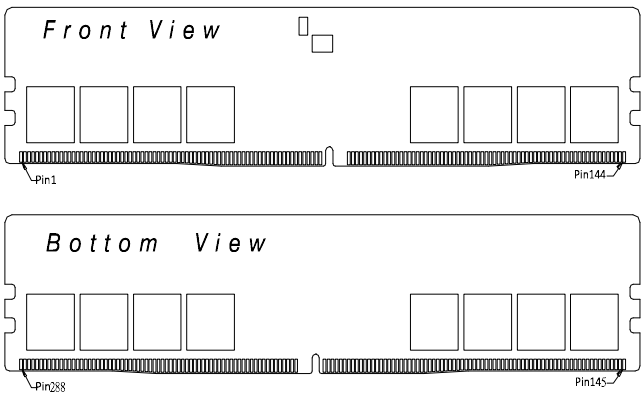
8GB by x16(1Rank)



16GB by x8(1Rank)



32GB byx8(2Rank)



Part No. Information

Part Number	Module Density	MT/s	Module Bandwidth	Module Organization	DRAM IC Composition	Ranks of Module
HLG4HK1-CE6UEC-EKAV	8GB	4800	38400GB/s	1Gx64	1Gbx16	1
HLH2HK1-C28NEC-AKAV	16GB	4800	38400GB/s	2Gx64	2Gbx8	1
HLI8HK1-C28NEC-CKAV	32GB	4800	38400GB/s	4Gx64	2Gbx8	2
HLG4MN1-CE6UEC-EKAV	8GB	5600	44800GB/s	1Gx64	1Gbx16	1
HLH2MN1-C28NEC-AKAV	16GB	5600	44800GB/s	2Gx64	2Gbx8	1
HLH2MN1-C28IEC-AKAV	16GB	5600	44800GB/s	2Gx64	2Gbx8	1
HLI8MN1-C28NEC-CKAV	32GB	5600	44800GB/s	4Gx64	2Gbx8	2
HLI8MN1-C28IEC-CKAV	32GB	5600	44800GB/s	4Gx64	2Gbx8	2

Key Parameters

MT/s	tCK (ns)	CAS Latency(ns)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP (tCK)
DDR5-4800	0.416	16	16	16	32	48	40-40-40
DDR5-5600	0.357	16	16	16	32	48	46-45-45

Address Table

		8GB (1Rx16)	16GB (1Rx8)	32GB (2Rx8)
Bank Address	# of Bank Groups	4 / 4 / 16	8 / 4 / 32	8 / 4 / 32
	BG Address	BG0~BG1	BG0~BG2	BG0~BG2
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		R0~R15	R0~R15	R0~R15
Column Address		C0~C9	C0~C9	C0~C9
Page size		2KB	1KB	1KB

Pin Assignments

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
1	VIN_BULK	145	VIN_BULK	40	Vss	184	Vss
2	RFU	146	VIN_BULK	41	DQ24_A	185	DQ26_A
3	RFU	147	PWR_GOOD	42	Vss	186	Vss
4	HSCL	148	HAS	43	DQ25_A	187	DQ27_A
5	HSDA	149	RGU	44	Vss	188	Vss
6	Vss	150	Vss	45	DM3_A_n	189	DQS3_A_c
7	RFU	151	PWR_EN	46	Vss	190	DQS3_A_t
8	Vss	152	RFU	47	DQ28_A	191	Vss
9	DQ0_A	153	Vss	48	Vss	192	DQ30_A
10	Vss	154	DQ2_A	49	DQ29_A	193	Vss
11	DQ1_A	155	Vss	50	Vss	194	DQ31_A
12	Vss	156	DQ3_A	51	CB0_A	195	Vss
13	DQS0_A_c	157	Vss	52	Vss	196	CB2_A
14	DQS0_A_t	158	DM0_A_n	53	CB1_A	197	Vss
15	Vss	159	Vss	54	Vss	198	CB3_A
16	DQ4_A	160	DQ6_A	55	DQS4_A_c	199	Vss
17	Vss	161	Vss	56	DQS4_A_t	200	ALERT_n
18	DQ5_A	162	DQ7_A	57	Vss	201	Vss
19	Vss	163	Vss	58	CS0_A_n	202	CS1_A_n
20	DQ8_A	164	DQ10_A	59	Vss	203	Vss
21	Vss	165	Vss	60	CA0_A	204	CA1_A
22	DQ9_A	166	DQ11_A	61	CA2_A	205	CA3_A
23	Vss	167	Vss	62	Vss	206	Vss
24	DM1_A_n	168	DQS1_A_c	63	CA4_A	207	CA5_A
25	Vss	169	DQS1_A_t	64	CA6_A	208	CA7_A
26	DQ12_A	170	Vss	65	Vss	209	Vss
27	Vss	171	DQ14_A	66	CA8_A	210	CA9_A
28	DQ13_A	172	Vss	67	CA10_A	211	CA11_A
29	Vss	173	DQ15_A	68	Vss	212	Vss
30	DQ16_A	174	Vss	69	CA12_A	213	RFU
31	Vss	175	DQ18_A	70	RFU	214	RFU
32	DQ17_A	176	Vss	71	Vss	215	Vss
33	Vss	177	DQ19_A	72	CK0_A_t	216	CK1_A_t
34	DQS2_A_c	178	Vss	73	CK0_A_c	217	CK1_A_c
35	DQS2_A_t	179	DM2_A_n	74	Vss	218	Vss
36	Vss	180	Vss	75	RFU	219	RFU
37	DQ20_A	181	DQ22_A	76	RFU	220	RFU
38	Vss	182	Vss	77	Vss	221	Vss
39	DQ21_A	183	DQ23_A	78	CK0_B_t	222	CK1_B_t

Pin Assignments (Continued)

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
79	CK0_B_c	223	CK1_B_c	112	DQ*_B	256	DQ10_B
80	Vss	224	Vss	113	Vss	257	Vss
81	RFU	225	RFU	114	DQ9_B	258	DQ11_B
82	CA12_B	226	RFU	115	Vss	259	Vss
83	Vss	227	Vss	116	DM1_B_n	260	DQS1_B_c
84	CA10_B	228	CA11_B	117	Vss	261	DQS1_B_t
85	CA8_B	229	CA9_B	118	DQ12_B	262	Vss
86	Vss	230	Vss	119	Vss	263	DQ14_B
87	CA6_B	231	CA7_B	120	DQ13_B	264	Vss
88	CA4_B	232	CA5_B	121	Vss	265	DQ15_B
89	Vss	233	Vss	122	DQ16_B	266	Vss
90	CA2_B	234	CA3_B	123	Vss	267	DQ18_B
91	CA0_B	235	CA1_B	124	DQ17_B	268	Vss
92	Vss	236	Vss	125	Vss	269	DQ19_B
93	CS0_B_n	237	CS1_B_n	126	DQS2_B_c	270	Vss
94	Vss	238	Vss	127	DQS2_B_t	271	DM2_B_n
95	RESET_n	239	DQS4_B_c	128	Vss	272	Vss
96	Vss	240	DQS4_C_t	129	Dq20_B	273	DQ22_B
97	CB0_B	241	Vss	130	Vss	274	Vss
98	Vss	242	CB2_B	131	DQ21_B	275	DQ23_B
99	CB1_B	243	Vss	132	Vss	276	Vss
100	Vss	244	CB3_B	133	DQ24_B	277	DQ26_B
101	DQ0_B	245	Vss	134	Vss	278	Vss
102	Vss	246	DQ2_B	135	DQ25_B	279	DQ27_B
103	DQ1_B	247	Vss	136	Vss	280	Vss
104	Vss	248	DQ3_B	137	DM3_B_n	281	DQS3_B_c
105	DQS0_B_c	249	Vss	138	Vss	282	DQS3_B_t
106	DQS_B_t	250	DM0_B_n	139	DQ28_B	283	Vss
107	Vss	251	Vss	140	Vss	284	DQ30_B
108	DQ4_B	252	DQ6_B	141	DQ29_B	285	Vss
109	Vss	253	Vss	142	Vss	286	DQ31_B
110	DQ5_B	254	DQ7_B	143	RFU	287	Vss
111	Vss	255	Vss	144	RFU	288	RFU

Pin Descriptions:

The pin description table below is a comprehensive list of all possible pins for DDR5 UDIMM/SODIMM devices. All pins listed may not be supported on a specific module.

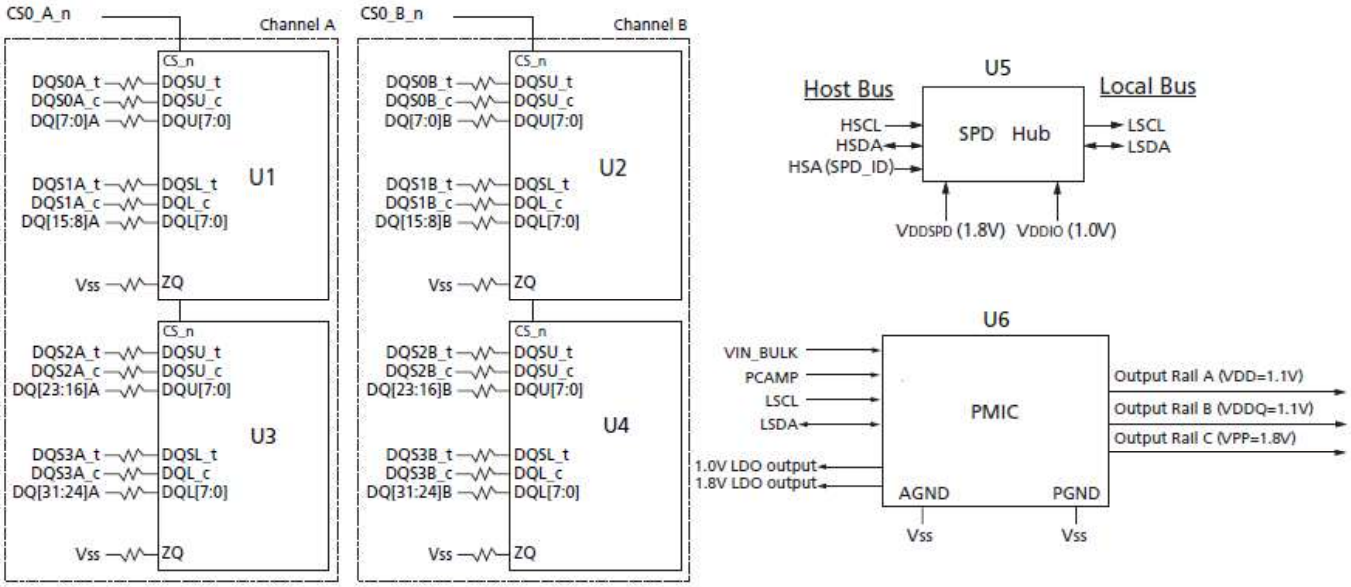
Pin Name	Type	I/O Level	Description
CA0_A ~ CA12_A CA0_B ~CA12_B	Input	VDDQ	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note that because some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during MODE REGISTER SET commands. The DDR5 component CA13 pin is strapped (connected) to eitherVSS or VDDQ depending on the strapped state of MIR.
CS0_A_n~ CS1_A_n CS0_B_n ~ CS1_B_n	Input	VDDQ	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down mode and self refresh mode. While not in self refresh mode the CS_n input buffer operates with the same ODT and VREF parameters as configured by the CA_ODT strap setting or mode register. When in self refresh, the CS_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDD.
DQ0_A ~ DQ31_A DQ0_B~DQ31_B	Input/ Output	VDDQ	Data Input/Output: Bidirectional data bus. If CRC is enabled via the mode register, THEN CRC CODE IS ADDED AT THE END OF DATA BURST. ANY DQ FROM DQ0–DQ3 may indicate the internal VREF level during test via mode register setting MR4 A4 =HIGH. Refer to the vendor-specific data sheets to determine which DQ is used.
CB0_A ~ CB3_A CB0_B ~CB3_B	Input/ Output	VDDQ	ECC Check Bits Input/Output: Bidirectional data bus. Only applicable on ECC SODIMM (SOEDIMM) or UDIMM (EUDIMM).
CK0_A_t, CK1_A_t CK0_B_t, CK1_B_t	Input	VDDQ	SDRAM Clocks CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CK0_A_c, CK1_A_c CK0_B_c, CK1_B_c			
DQS0_A_t~DQS4_A_t DQS0_B_t~DQS4_B_t	Input/ Output	VDDQ	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM only supports differential data strobe. It does not support single-ended strobe.
DQS0_A_c ~DQS4_A_c DQS0_B_c ~DQS4_B_c			
DM0_A_n ~DM3_A_n DM0_B_n~DM3_B_n	Input	VDDQ	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM function is shared with TDQS on x8 devices. The function of DM_n is enabled by MR5:OP[5] = 1. Refer to DDR5 component data sheet specification for further detail.
VIN_BULK	Supply		External Power Supply: 5V, 4.25V (min), 5.5V (max)

Pin Descriptions (Continued)

Pin Name	Type	I/O Level	Description
PWR_GOOD	Input Output	VDDQ	Power Good Indicator: Open drain output. The PMIC ensures this pin HIGH when VIN_Bulk input supply, as well as all enabled output buck regulators and all LDO regulators tolerance threshold is maintained as configured in the appropriate register. The PMIC drives this pin LOW when VIN_Bulk input goes below the threshold or when any of the enabled output buck regulator exceeds the thresholds configured in the appropriate register or when any LDO output regulator exceeds the threshold configured in the appropriate register. As an input, the PMIC disables its output regulator when this pin is LOW. The LDO outputs remain on.
HSCL	Input	VOUT_1.8V or VOUT_1.0V	Host Sideband Bus Clock: Bus clock used to strobe data into HUB device. When open drain, a pull-up resistor is required on the system motherboard.
HSDA	Input/ Output	VOUT_1.8V or VOUT_1.0V	Host Sideband Bus Data:I2C/I3C-Basic data. When open drain, a pull-up resistor is required on the system motherboard.
HSA	Input	GND	Host Sideband Bus Device ID: Address input to a hub or other client device to distinguish between identical devices in the I3C basic address range. Tied to GND,HSA has different resistor values on the motherboard to identify DIMM slot address. Refer to the SPD Hub spec for more information.
VSS	Supply		Ground
PWR_EN	Input		PMIC Enable: When this pin is HIGH, the PMIC turns on the regulator. When this pin is LOW, the PMIC turns off the regulator. This signal is connected to the PMIC's VR_EN pin.
RESET_n	CMOS Input	VDDQ	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDDQ.
ALERT_n	Output	VDDQ	Alert: If there is an error in CRC, then ALERT_n drives LOW for the period time interval and returns HIGH. During connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In the case where this pin is not connected, ALERT_n must be bonded to VDDQ on the system board.
RFU			Reserved for future use. No on DIMM electrical connection is present

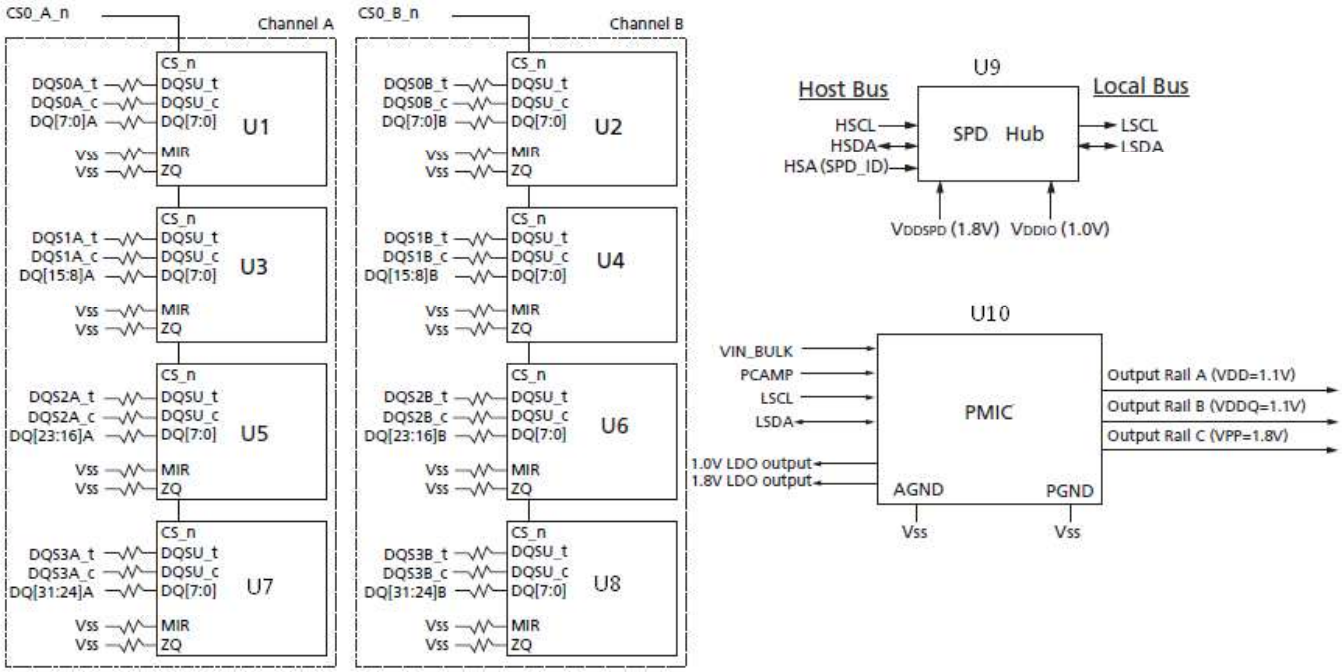
Functional Block Diagram:

8GB 1Gx64 (1Rank by x16)



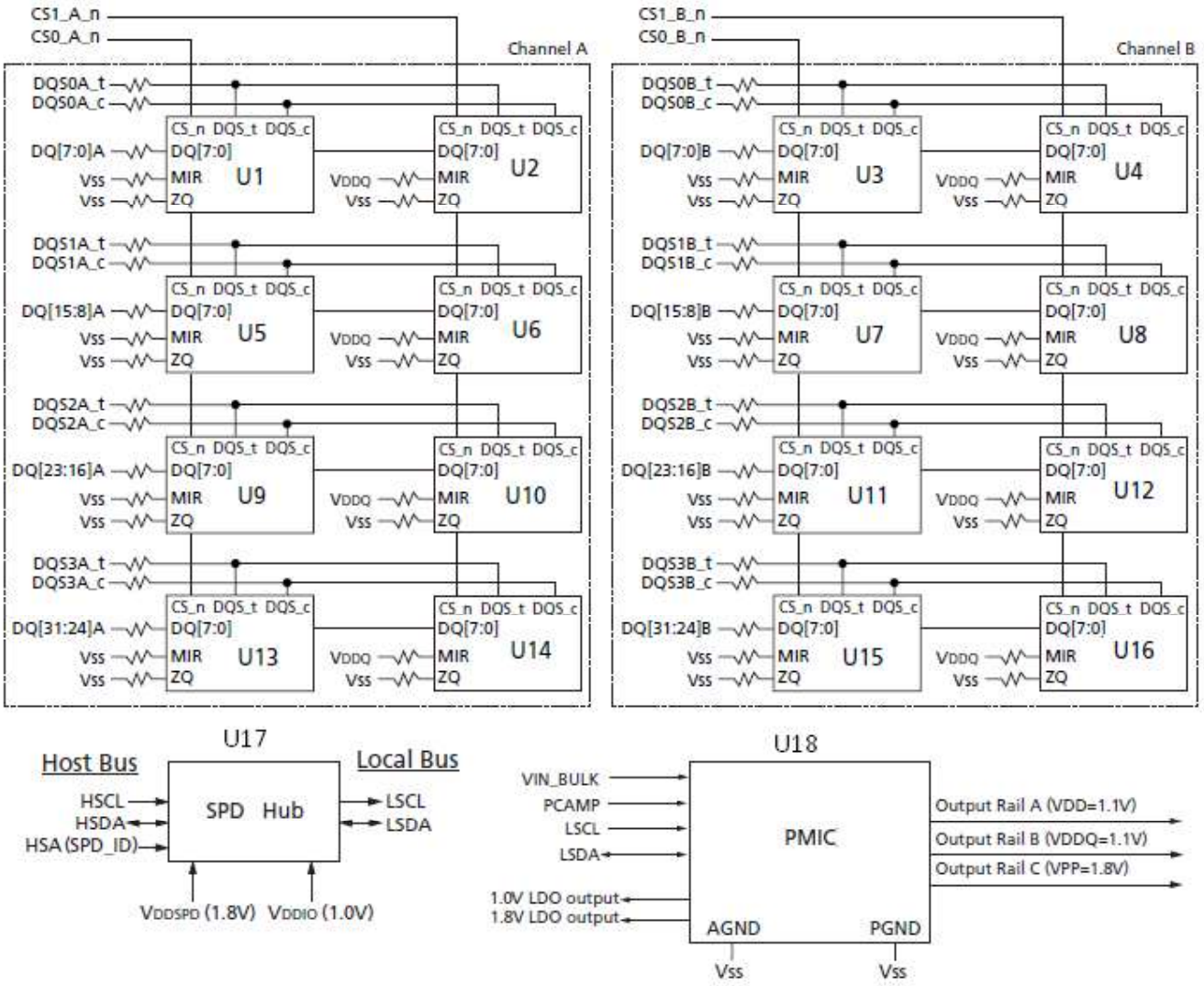
Note: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

16GB 2Gx64 (1Rank by x8)



Note: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

32GB 4Gx64 (2Rank by x8)



Note: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Electrical Specifications:

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	VDD supply voltage relative to VSS	-0.3 ~ 1.5	V	1,3
VDDQ	VDDQ supply voltage relative to VSS	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to VSS	-0.3 ~ 2.1	V	4
VIN, VOUT	Voltage on any pin relative to VSS	-0.3 ~ 1.5	V	1,3,5

Note:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times. When VDD and VDDQ are less than 500 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.
5. Overshoot area above 1.5 V is specified in Section 8.3.4, Section 8.3.5, and Section 8.3.6.

Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Device Supply Voltage	1.067(-3%)	1.1	1.166(+6%)	V
VDDQ	Supply Voltage for I/O	1.067(-3%)	1.1	1.166(+6%)	V
VPP	Core Power Voltage	1.746(-3%)	1.8	1.908(+6%)	V

Thermal Characteristics:

Symbol	Parameter/Condition	Value	Unit	Note
TC	Commercial operating case temperature	0 to 85	°C	1,2,3
TC		>85 to 95	°C	1,2,3,4
TOPER	Normal operating temperature range	0 to 85	°C	5
TOPER	Extended temperature operating range (optional)	>85 to 95	°C	5
TSTG	Non-operating storage temperature	–55 to 100	°C	6

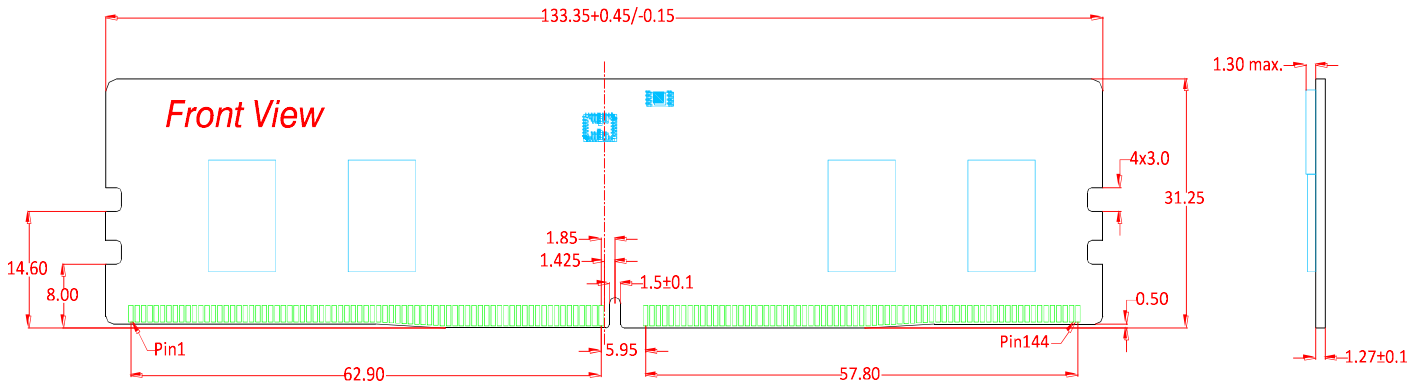
Notes:
1. Maximum operating case temperature; TC is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum TC during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum TC during operation.
4. If TC exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate.
5. The refresh rate must double when 85°C < TOPER ≤ 95°C.
6. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.

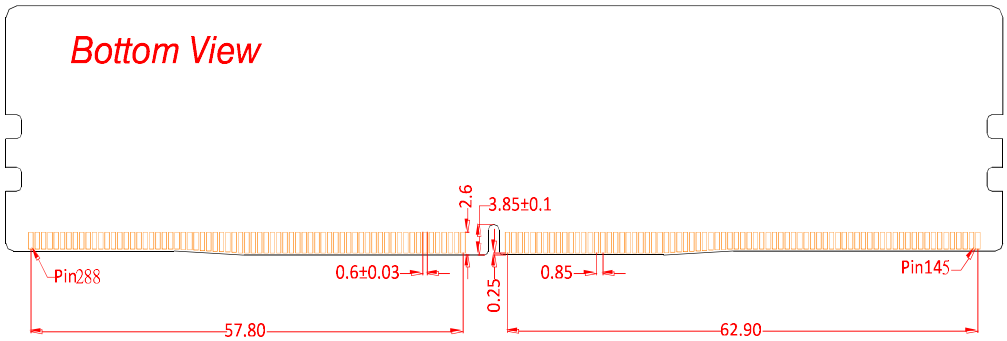
IDD Specifications:

Symbol	Parameter	8GB (1R byx16)		16GB (1R byx8)		32GB (2R byx8)		Unit
		4800	5600	4800	5600	4800	5600	
IDD0	Operating one bank ACTIVATE-PRECHARGE current	98	108	139	154	247	222	mA
IDDF	Operating four bank ACTIVATE-PRECHARGE current	172	176	220	229	328	297	mA
IDD2N	Precharge standby current	74	84	109	125	219	206	mA
IDD2NT	Precharge standby non-target command	166	135	243	200	370	278	mA
IDD2P	Precharge power-down current	65	77	93	113	187	181	mA
IDD3N	Active standby current	81	92	124	139	249	239	mA
IDD3P	Active power-down current	75	84	110	127	221	214	mA
IDD4R	Operating burst read current	537	636	652	777	757	892	mA
IDD4W	Operating burst write current	778	909	890	1025	993	1141	mA
IDD4WC	Operating burst write with write CRC current	695	827	803	911	907	1028	mA
IDD5F	Burst refresh (fine granularity refresh mode) current	248	254	251	750	550	830	mA
IDD5B	Burst refresh (normal refresh mode) current	160	240	274	719	373	790	mA
IDD5C	Burst refresh (same bank refresh mode) current	113	135	190	297	290	349	mA
IDD6N	Self refresh current	31	48	60	83	119	152	mA
IDD7	Operating bank interleave read current	634	708	722	1186	825	1260	mA
IDD8	Maximum power saving deep power down mode current	23	39	43	66	86	114	mA

Module Dimensions

8GB 1Gx64 (1Rank by x16)

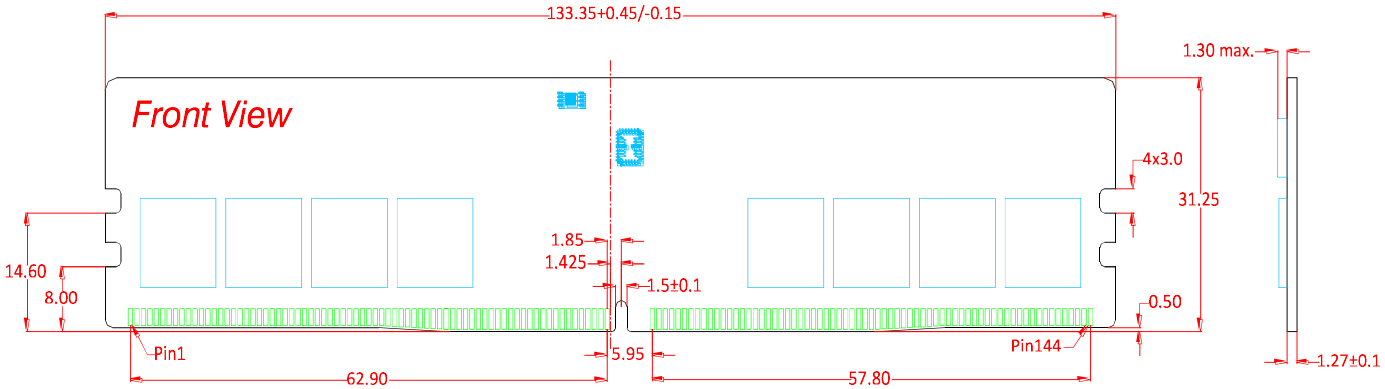


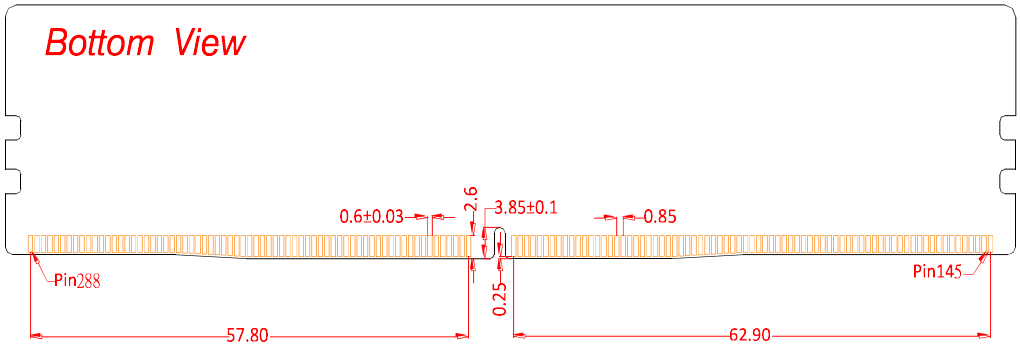


Notes:

1. All dimensions are in millimeters.
2. Tolerance on all dimensions is ±0.15mm unless otherwise specified
3. The dimensional diagram is for reference only.

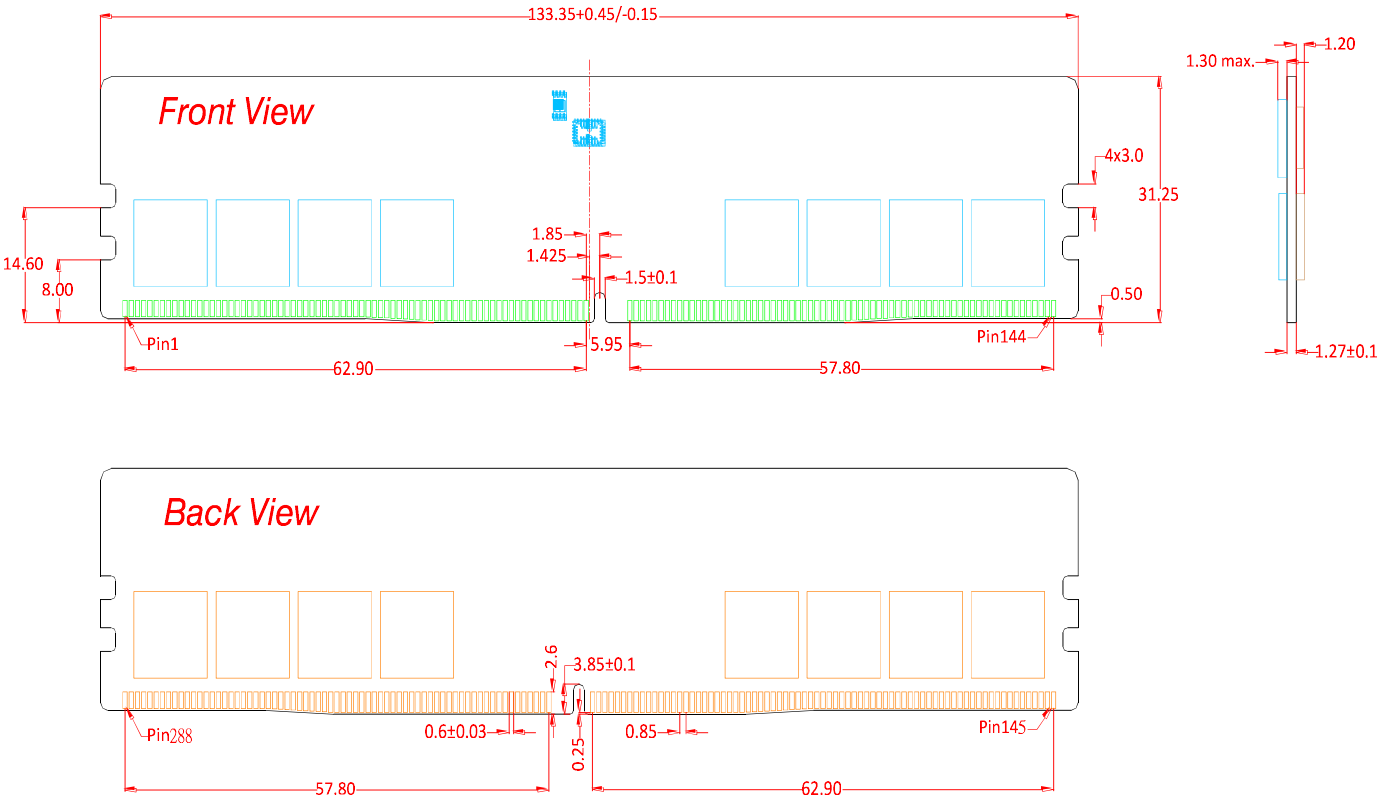
16GB 2Gx64 (1Rank by x8)





Notes: 1. All dimensions are in millimeters.
2. Tolerance on all dimensions is ±0.15mm unless otherwise specified
3. The dimensional diagram is for reference only.

32GB 4Gx64 (2Rank by x8)



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