Memory Module Datasheet

DDR5-5600 SODIMM
Based on 16Gb P-die

Jul 04th, 2024

Rev 1.0

Ordering Information

Part Number	Description	Device Vendor
ZMS5WMC3C1J0B46SPG	8GB SODIMM (1Gx64) 1Rx16, DDR5-5600 (46-45-45), 1Gx16 based IC, 262-pin, 1.1V, 30.00 mm, Halogen-Free (RoHS Compliant)	IC Zilia P/N ZDRPAH6Y16XCWM1N9T Samsung IC ref. P/N K4RAH165VP-BCWM, Samsung module ref. P/N M425R1GB4PB0-CWMOD
ZMS5WMC8C2J0B46SPG	16GB SODIMM (2Gx64) 1Rx8, DDR5-5600 (46-45-45), 2Gx8 based IC, 262-pin, 1.1V, 30.00 mm, Halogen-Free (RoHS Compliant)	IC Zilia P/N ZDRPAH2Y08XCWM8N9T Samsung IC ref. P/N K4RAH086VP-BCWM Samsung module ref. P/N M425R2GA3PB0-CWMOD
ZMS5WMC8C4J0B46SPG	32GB SODIMM (4Gx64) 2Rx8, DDR5-5600 (46-45-45), 2Gx8 based IC, 262-pin, 1.1V, 30.00 mm, Halogen-Free (RoHS Compliant)	IC Zilia P/N ZDRPAH2Y08XCWM8N9T Samsung IC ref. P/N K4RAH086VP-BCWM, Samsung module ref. P/N M425R4GA3PB0-CWMOD

Part Number Decoder

Z	M	S	5	W	M	C	#	C	#	J	0	B	4	6	S	P	G
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

1	**Module Manufacturer** **Z:** Zilia Technologies
2	**Product Identification** **M:** Memory Module (RoHS & Halogen-Free & Sb-Free)
3	**DIMM Type** **S:** Small Outline DIMM
4	**DRAM Component Type** **5:** DDR5 SDRAM
5~6	**Speed** **WM:** DDR5-5600B (46-45-45)
7	**Temperature & Power** **C:** Commercial Temp (0°~85°C) & Normal Power
8	**DRAM Bit Organization** **3:** x16 **8:** x8
9	**DRAM Package Type** **C:** FBGA(Flip-Chip)
10~11	**Module Depth** **1J**: 1Gb **2J**: 2Gb **4J**: 4Gb
12	**PCB Revision** **0:** None
13	**PMIC & RCD Information** **B:** RNS
14~15	**Module Pinout/Data Width** **46:** 262-Pin x64
16	**Module Design** **S:** Samsung
17	**DRAM IC Generation** **P:** P-die
18	**Internal Code** **G**

Revision History

Date	Description
Jul 04th, 2024	Initial release.

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1.0 DDR5 SMALL OUTLINE DIMM ORDERING INFORMATION

[Table 1] Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	Height
ZMS5WMC3C1J0B46SPG	8GB	1Gx64	1Gx16(ZDRPAH6Y16XCWM1N9T) * 4	1	30mm
ZMS5WMC8C2J0B46SPG	16GB	2Gx64	2Gx8(ZDRPAH2Y08XCWM8N9T) * 8	1	30mm
ZMS5WMC8C4J0B46SPG	32GB	4Gx64	2Gx8(ZDRPAH2Y08XCWM8N9T) * 16	2	30mm

2.0 KEY FEATURES

[Table 2] Speed Bin

Speed	DDR5-4400	DDR5-4800	DDR5-5200	DDR5-5600	Unit
	36-36-36	40-39-39	42-42-42	46-45-45	
tCK(min)	0.454	0.416	0.384	0.357	ns
CAS Latency	36	40	42	46	nCK
tRCD(min)	16.000	16.000	16.000	16.000	ns
tRP(min)	16.000	16.000	16.000	16.000	ns
tRAS(min)	32.000	32.000	32.000	32.000	ns
tRC(min)	48.000	48.000	48.000	48.000	ns

- JEDEC standard compliant.
- VDD = VDDQ = 1.1V (1.067V(- 3%) ~ 1.166V(+6%)).
- VPP = 1.8V (1.746 (-3%) ~ 1.908 (+6%).
- 2000MHz fCK for 4000Mb/sec/pin, 2200MHz fCK for 4400Mb/sec/pin, 2400MHz fCK for 4800Mb/sec/pin. 2600MHz fCK for 5200Mb/sec/pin 2800MHz fCK for 5600Mb/sec/pin.
- 32 Banks (8 Bank Groups).
- Programmable CAS Latency (posted CAS): 22,26,28,30,32,36,40,42,46,50
- Programmable CAS Write Latency (CWL) = CL-2.
- 16-bit prefetch.
- Burst Length: 16 by default. 8 with tCCD=8, which does not allow gapless READ or WRITE, where BC8 and BL32 refer to CA5 BL*=L.
- Bi-directional Differential Data-Strobe.
- Internal ZQ calibration via Multi-Purpose Command (MPC) - ZQcal start and ZQcal Latch.
- On Die Termination (ODT) via Mode Register setting : RTT_PARK, RTT_WR, RTT_NOM_WR, RTT_NOM_RD.
- Average Refresh period 3.9us at lower than TCASE 85°C, 1.95us at 85°C < TCASE < 95 °C.
- Connectivity Test Mode (TEN) is supported.
- Asynchronous Reset.

3.0 ADDRESS CONFIGURATION

[Table 3] Address Information

Configuration		2Gb x8	1Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	4 / 4 / 16
Row ddress		R0~R15	R0~R15
Column Address		C0~C9	C0~C9
Page size		1KB	2KB

4.0 SMALL OUTLINE DIMM PIN INFORMATION

[Table 4] PIN Configuration

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	VIN_BULK	2	HSA	99	CB2_A	100	DQS4_A_c	195	DQ6_B	196	VSS
3	VIN_BULK	4	HSCL	101	VSS	102	DQS4_A_t	197	VSS	198	DQ7_B
5	RFU	6	HSDA	103	CB3_A	104	VSS	199	DQ8_B	200	VSS
7	PWR_GOOD	8	PWR_EN	105	VSS	106	CS0_A_n	201	VSS	202	DQ9_B
9	VSS	10	VSS	107	CA0_A	108	ALERT_n	203	DQ10_B	204	VSS
11	DQ0_A	12	DQ1_A	109	CA1_A	110	CS1_A_n	205	VSS	206	DQ11_B
13	VSS	14	VSS	111	VSS	112	VSS	207	DQS1_B_c	208	VSS
15	DQ2_A	16	DQ3_A	113	CA2_A	114	CA3_A	209	DQS1_B_t	210	DM1_B_n
17	VSS	18	VSS	115	CA4_A	116	CA5_A	211	VSS	212	VSS
19	DM0_A_n	20	DQS0_A_c	117	VSS	118	VSS	213	DQ12_B	214	DQ13_B
21	VSS	22	DQS0_A_t	119	CA6_A	120	CA7_A	215	VSS	216	VSS
23	DQ4_A	24	VSS	121	CA8_A	122	CA9_A	217	DQ14_B	218	DQ15_B
25	VSS	26	DQ5_A	123	VSS	124	VSS	219	VSS	220	VSS
27	DQ6_A	28	VSS	125	CA10_A	126	CA11_A	221	DQ16_B	222	DQ17_B
29	VSS	30	DQ7_A	KEY				223	VSS	224	VSS
31	DQ8_A	32	VSS	127	CA12_A	128	RFU	225	DQ18_B	226	DQ19_B
33	VSS	34	DQ09_A	129	VSS	130	VSS	227	VSS	228	VSS
35	DQ10_A	36	VSS	131	CK0_A_t	132	CK1_A_t	229	DM2_B_n	230	DQS2_B_c
37	VSS	38	DQ11_A	133	CK0_A_c	134	CK1_A_c	231	VSS	232	DQS2_B_t
39	DQS1_A_c	40	VSS	135	VSS	136	VSS	233	DQ20_B	234	VSS
41	DQS1_A_t	42	DM1_A_n	137	CK0_B_t	138	CK1_B_t	235	VSS	236	DQ21_B
43	VSS	44	VSS	139	CK0_B_c	140	CK1_B_c	237	DQ22_B	238	VSS
45	DQ12_A	46	DQ13_A	141	VSS	142	VSS	239	VSS	240	DQ23_B
47	VSS	48	VSS	143	RFU	144	CA12_B	241	DQ24_B	242	VSS
49	DQ14_A	50	DQ15_A	145	CA11_B	146	CA10_B	243	VSS	244	DQ25_B
51	VSS	52	VSS	147	VSS	148	VSS	245	DQ26_B	246	VSS
53	DQ16_A	54	DQ17_A	149	CA9_B	150	CA8_B	247	VSS	248	DQ27_B
55	VSS	56	VSS	151	CA7_B	152	CA6_B	249	DQS3_B_c	250	VSS
57	DQ18_A	58	DQ19_A	153	VSS	154	VSS	251	DQS3_B_t	252	DM3_B_n
59	VSS	60	VSS	155	CA5_B	156	CA4_B	253	VSS	254	VSS
61	DM2_A_n	62	DQS2_A_c	157	CA3_B	158	CA2_B	255	DQ28_B	256	DQ29_B
63	VSS	64	DQS2_A_t	159	VSS	160	VSS	257	VSS	258	VSS
65	DQ20_A	66	VSS	161	CS0_B_n	162	CA1_B	259	DQ30_B	260	DQ31_B
67	VSS	68	DQ21_A	163	RESET_n	164	CA0_B	261	VSS	262	VSS
69	DQ22_A	70	VSS	165	CS1_B_n	166	VSS				
71	VSS	72	DQ23_A	167	VSS	168	CB0_B				
73	DQ24_A	74	VSS	169	DQS4_B_c	170	VSS				
75	VSS	76	DQ25_A	171	DQS4_B_t	172	CB1_B				
77	DQ26_A	78	VSS	173	VSS	174	VSS				
79	VSS	80	DQ27_A	175	CB3_B	176	CB2_B				
81	DQS3_A_c	82	VSS	177	VSS	178	VSS				
83	DQS3_A_t	84	DM3_A_n	179	DQ0_B	180	DQ1_B				
85	VSS	86	VSS	181	VSS	182	VSS				
87	DQ28_A	88	DQ29_A	183	DQ2_B	184	DQ3_B				
89	VSS	90	VSS	185	VSS	186	VSS				
91	DQ30_A	92	DQ31_A	187	DM0_B_n	188	DQS0_B_c				
93	VSS	94	VSS	189	VSS	190	DQS0_B_t				
95	CB0_A	96	CB1_A	191	DQ4_B	192	VSS				
97	VSS	98	VSS	193	VSS	194	DQ5_B				

[Table 5] PIN Description

Pin Name	Description
CA0_A – CA12_A, CA0_B – CA12_B	SDRAM Command/Address bus
CS0_A_n – CS1_A_n, CS0_B_n – CS1_B_n	SDRAM Chip Select
DQ0_A – DQ31_A, DQ0_B – DQ31_B	DIMM memory data bus
CB0_A – CB3_A, CB0_B – CB3_B	DIMM ECC check bits
DQS0_A_t – DQS4_A_t, DQS0_B_t – DQS4_B_t	SDRAM data strobes (positive line of differential pair)
DQS0_A_c – DQS4_A_c, DQS0_B_c – DQS4_B_c	SDRAM data strobes (negative line of differential pair)
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	SDRAM data masks
CK0_A_t, CK1_A_t, CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)
CK0_A_c, CK1_A_c, CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)

Pin Name	Description
HSCL	SidebandBus clock
HSDA	SidebandBus data
HSA	SidebandBus address
ALERT_n	SDRAM ALERT_n
RESET_n	Set DRAMs to a Known State
VIN_BULK	5V power input supply to the PMIC for analog circuits
VSS	Power supply return (ground)
PWR_GOOD	Power good indicator
PWR_EN	PMIC Enable
RFU	Reserved for future use

NOTE :
1) DDR5 SO-DIMM has 2 channels (channel-A and channel-B) of signal bus.
The signals with suffix: _A (e.g. DQ0_A) are for channel-A, and the signals with suffix: _B (e.g. DQ0_B) are for channel-B

5.0 INPUT/OUTPUT FUNCTIONAL DESCRIPTION

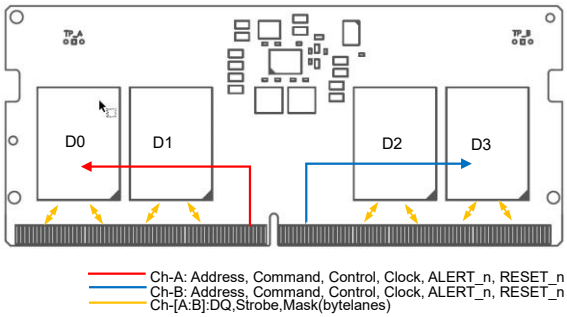
[Table 6] Input/Output Function Description

Symbol	Type	I/O Level	Function
CK0_A_t, CK0_A_c, CK1_A_t, CK1_A_c, CK0_B_t, CK0_B_c, CK1_B_t, CK1_B_c	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A - CA12_A, CA0_B –CA12_B	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins may not be interchanged between devices on the same bus.
CS0_A_n – CS1_A_n, CS0_B_n – CS1_B_n	Input	VDD	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks.
DQ0_A – DQ31_A, DQ0_B – DQ31_B	Input/Output	VDDQ	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
CB0_A – CB3_A, CB0_B – CB3_B	Input/Output	VDDQ	DIMM ECC check bits.
DQS0_A_t – DQS4_A_t, DQS0_A_c – DQS4_A_c, DQS0_B_t – DQS4_B_t, DQS0_B_c – DQS4_B_c	Input/Output	VDDQ	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	Input	VDDQ	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1.
ALERT_n	Input/Output	VDD	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDDQ on board.
RESET_n	Input	VDD	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ,
HSCL	Input	1.0V	Host SidebandBus bus clock, supplied by the master.
HSDA	Input/Output	1.0V	Host SidebandBus data, connected from the master to hubs or host bus client devices.
HSA	Input	2.1V max	Host SidebandBus bus device ID address pin; input to a hub or other client device to distinguish between identical devices in the I3C Basic address range.
RFU			Reserved for Future Use. No on DIMM electrical connection is present.
PWR_GOOD	Input/Output	Open Drain	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as all enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or when any of the enabled switch output regulators exceed the threshold configured in the appropriate register or any LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.
PWR_EN	Input	3.3V	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This signal is connected to PMIC's VR_EN pin.
VIN_BULK	Supply	5V	5 V power input supply to the PMIC for analog circuits.
VSS	Supply		Ground.

6.0 FUNCTION BLOCK DIAGRAM

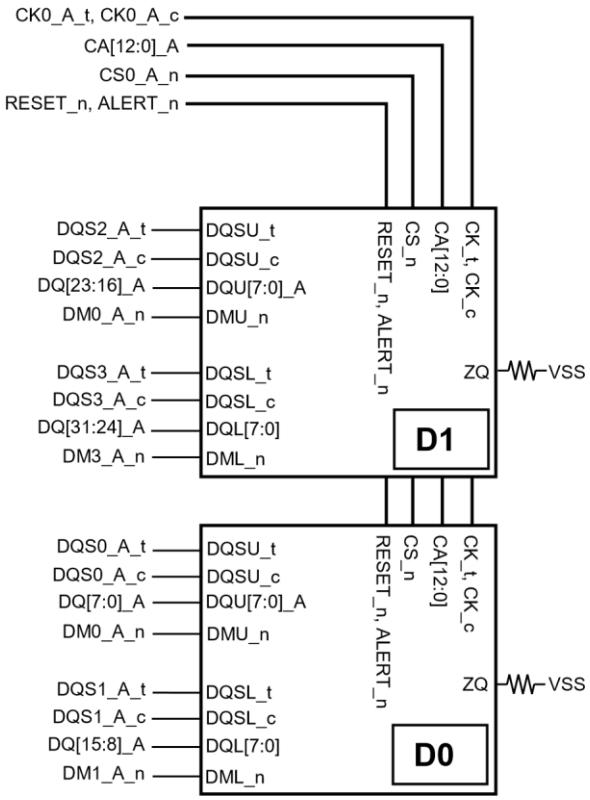
6.1 8GB, x64 DIMM (Populated as 1 rank of x16 DDR5 SDRAMs)

6.1.1 8GB, x64 DIMM (Populated as 1 rank of x16 DDR5 SDRAMs) – Part 1 of 4



6.1.2 8GB, x64 DIMM (Populated as 1 rank of x16 DDR5 SDRAMs) – Part 2 of 4

Channel A



NOTE :

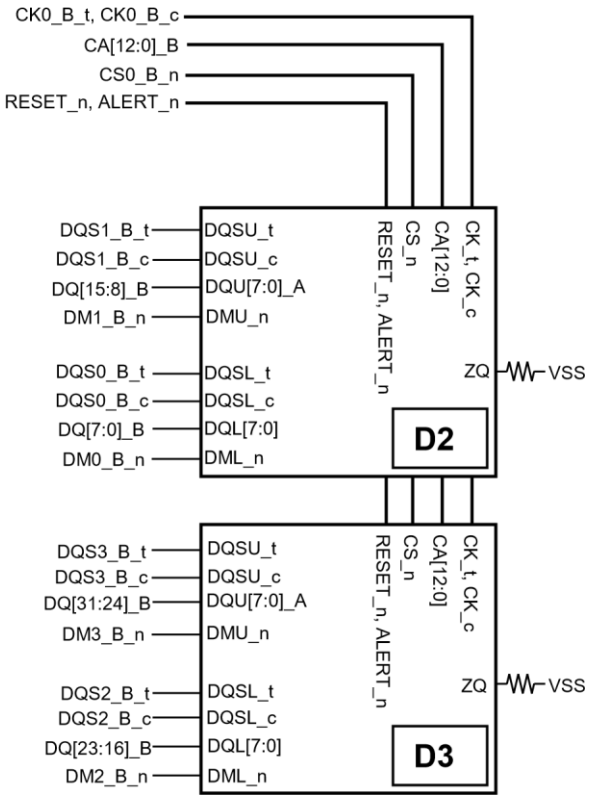
1) Unless otherwise noted resistors are 15Ω ± 5% 2) ZQ resistors are 240Ω ± 1%.

3) CK1_[A:B]_t/c edge pin signals are each terminated with 33Ω ± 5% resistor to VSS.

4) CS1_[A:B]_n edge pin signals are each terminated with 39Ω ± 5% resistor to VSS.

6.1.3 8GB, x64 DIMM (Populated as 1 rank of x16 DDR5 SDRAMs) – Part 3 of 4

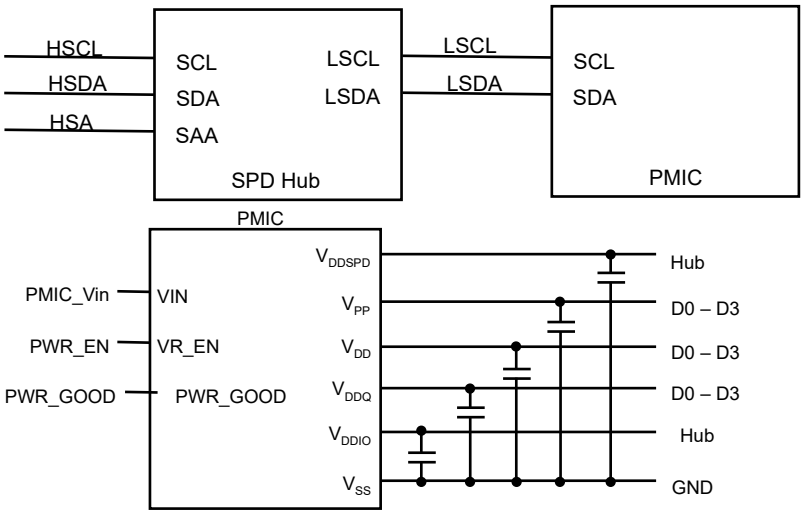
Channel B



NOTE :

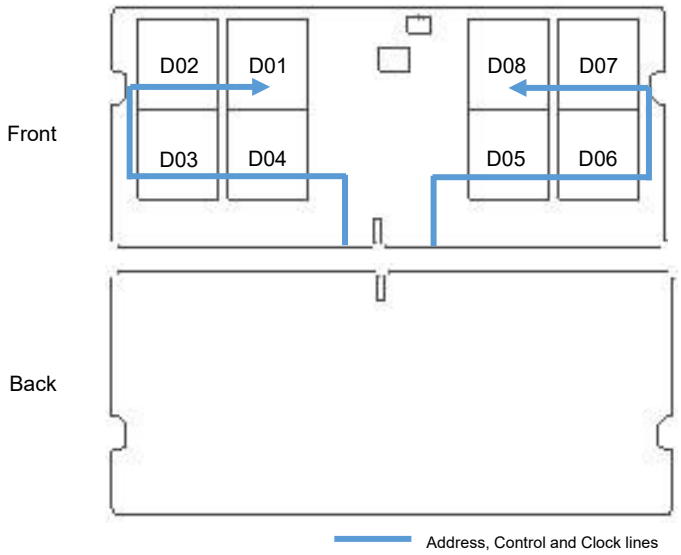
1) Unless otherwise noted resistors are
15Ω ± 5% 2) ZQ resistors are 240Ω ± 1%.
3) CK1_[A:B]_t/c edge pin signals are each terminated with 33Ω ± 5% resistor to VSS.
4) CS1_[A:B]_n edge pin signals are each terminated with 39Ω ± 5% resistor to VSS.

6.1.4 8GB, x64 DIMM (Populated as 1 rank of x16 DDR5 SDRAMs) – Part 4 of 4



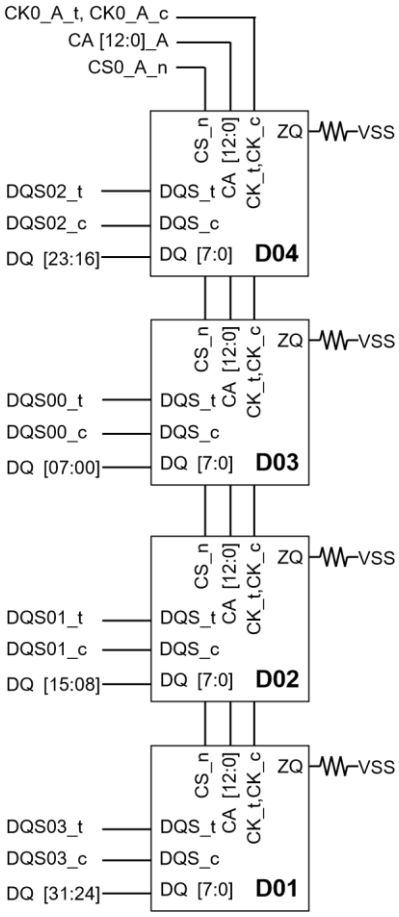
6.2 16GB, x64 DIMM (Populated as 1 rank of x8 DDR5 SDRAMs)

6.2.1 16GB, x64 DIMM (Populated as 1 rank of x8 DDR5 SDRAMs) - Part 1 of 4



6.2.2 16GB, x64 DIMM (Populated as 1rank of x8 DDR5 SDRAMs) - Part 2 of 3

Channel A

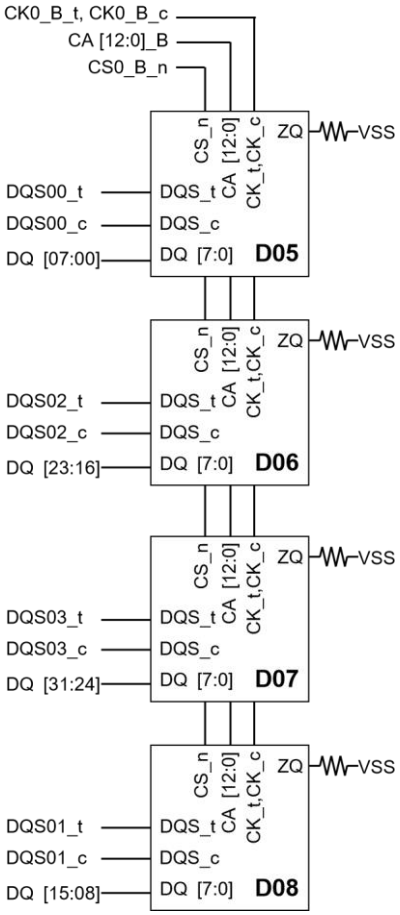


NOTE :

1) ZQ resistors are 240 Ω ± 1%.

6.2.3 16GB, x64 DIMM (Populated as 1rank of x8 DDR5 SDRAMs) - Part 3 of 3

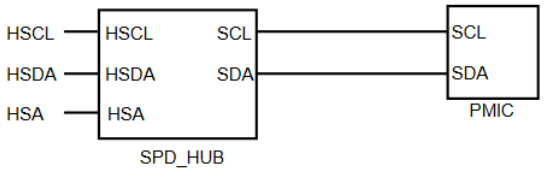
Channel B

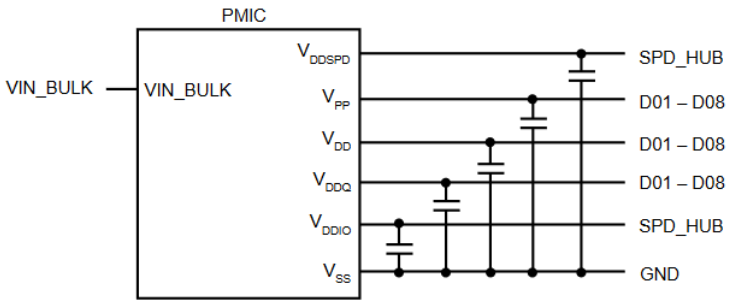


NOTE :

1) ZQ resistors are 240 Ω ± 1%.

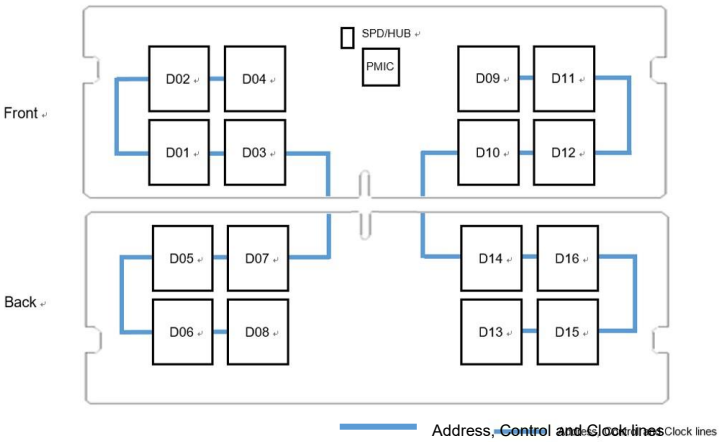
6.2.4 16GB, x64 DIMM (Populated as 1 rank of x8 DDR5 SDRAMs) - Part 4 of 4





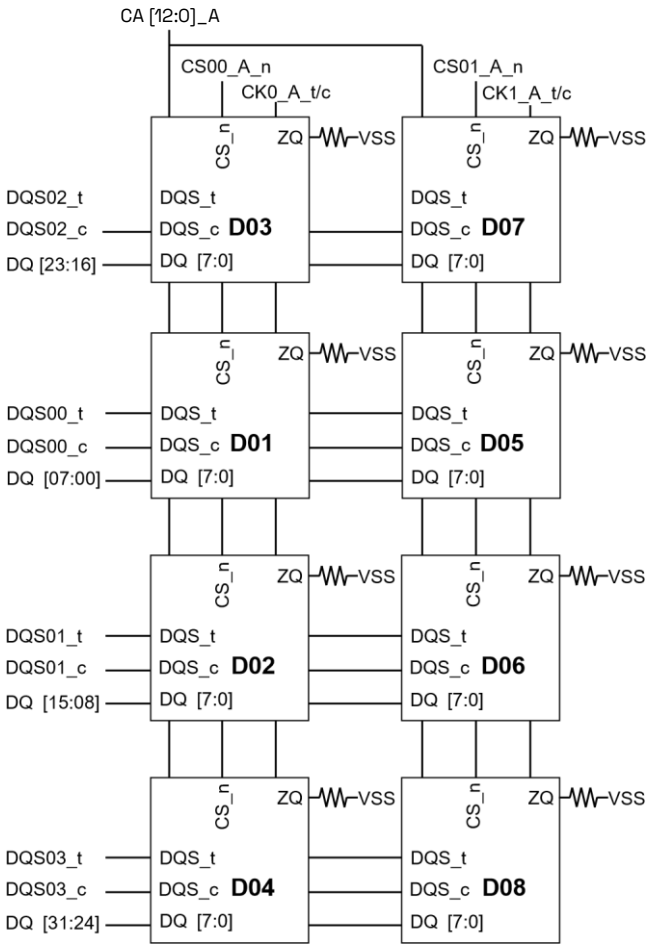
6.3 32GB, x64 DIMM (Populated as 2 ranks of x8 DDR5 SDRAMs)

6.3.1 32GB, x64 DIMM (Populated as 2 ranks of x8 DDR5 SDRAMs) - Part 1 of 4



6.3.2 32GB, x64 DIMM (Populated as 2 ranks of x8 DDR5 SDRAMs) - Part 2 of 4

Channel A

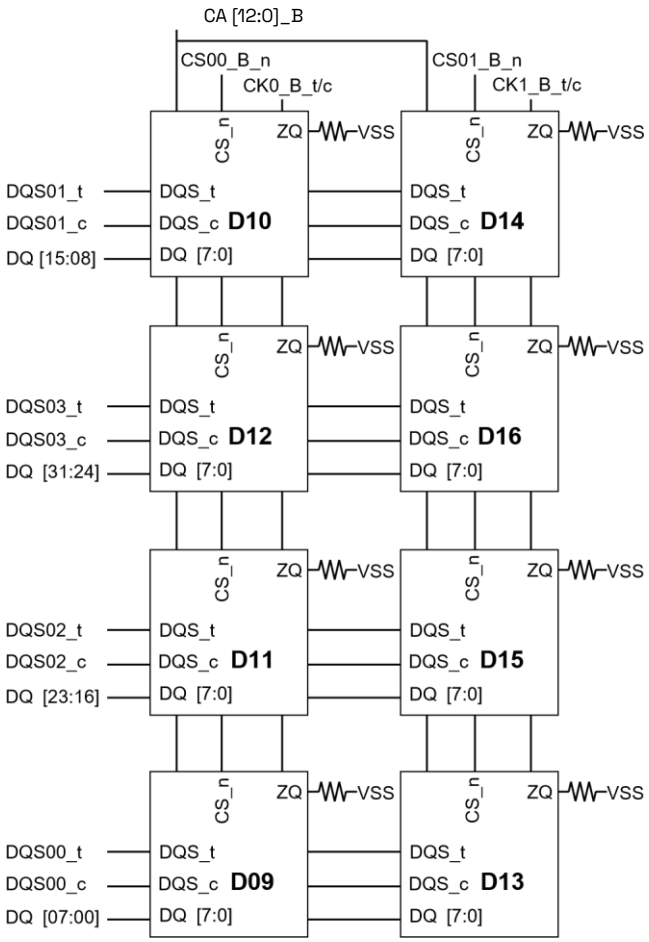


NOTE :

1) ZQ resistors are 240 Ω ± 1%.

6.3.3 32GB, x64 DIMM (Populated as 2 ranks of x8 DDR5 SDRAMs) - Part 3 of 4

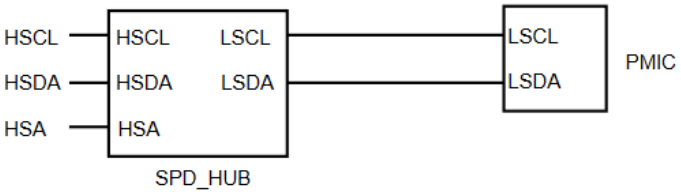
Channel B

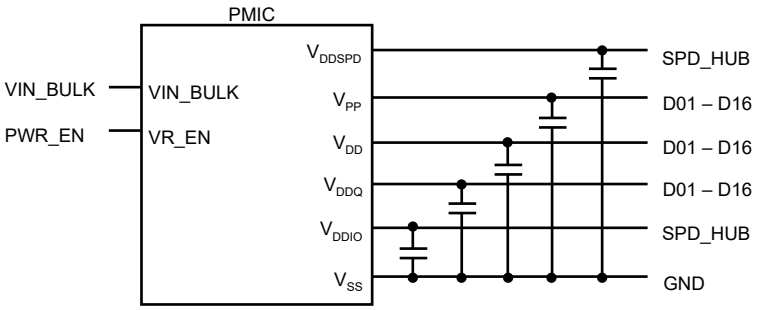


NOTE :

1) ZQ resistors are 240 Ω ± 1%.

6.3.4 32GB, x64 DIMM (Populated as 2 ranks of x8 DDR5 SDRAMs) - Part 4 of 4





7.0 AC & DC OPERATING CONDITIONS

7.1 DIMM Voltage Requirements

The DIMM input voltage requirements and the SDRAM voltage requirements are not identical. The DIMM voltage requirements must meet the PMIC input voltage requirements. The PMIC output voltage requirements must meet the SDRAM voltage requirements. There must be some allowance for a small voltage drop across the DIMM for both supply voltages and PMIC output voltages. Table 15 defines the requirements from the Host at the DIMM socket and at the post-PMIC SDRAM pin. Some modules have lower current requirements. Each specific module configuration must meet the PMIC 50x0, SDRAM, DDR5RCDxx and DDR5DBxx voltage requirements for its worst case supply currents

[Table 15] DDR5 SODIMM DC Operating Voltage [1,2,3]

Symbol	Parameter	Voltage Rating (Volts)			Maximum Expected Current (Amps)	Power State
		Minimum	Typical	Maximum		
VIN_BULK	Host Supply Voltage	4.25	5.0	5.5	2A	Operational
SWA, SWB	PMIC Output Supply Voltage	-	1.1	-	6	Operational
SWA+SWB	PMIC Output Supply Voltage	-	1.1	-	12	Operational
SWC	PMIC Output Supply Voltage	-	1.8	-	2	Operational
1.8V LDO	PMIC Output Supply Voltage	-	1.8	-	0.025	Operational
1.0V LDO	PMIC Output Supply Voltage	-	1.0	-	0.020	Operational

NOTE:

1) During first power on, the input voltage supply must reach minimum 4.25 V for PMIC to detect valid input supply. 2) The ramp up rate between 300 mV and 4.0 V.
3) The ramp down rate between 4.0 V and 300 mV.
4) The area under the curve above VIN_Bulk = TBD V. VIN_Bulk_AC spec must also be satisfied.
5) The minimum input current requirement is to deliver the maximum output current on VOUT_1.8V and VOUT_1.0V LDO plus the current
6) VIN_Bulk = 5.0 V. Measured at room temperature. All circuitry including output regulators and LDOs are off. VR_EN signal is static
7) VIN_Bulk = 5.0 V. Measured at room temperature. All output regulators and LDOs are on with 0 A output load. VR_EN signal is static 8) 20 MHz bandwidth limited measurement for all voltages in the table
9) Voltages are measured at the DIMM gold fingers and at PMIC output pins
10) The SDRAM specification must be met and take precedence over this document
11) Maximum current establishes the platform maximum current regulation point. It provides a data point for DIMM developers to set power plane impedances 12) Typical voltage is platform dependent. This is a suggested value only

7.2 Recommended Operating Temperature Ranges

[Table 16] Recommended Operating Temperature Ranges

Parameter/Condition	Device Rating	Symbol	Min	Normal	Extended
Commercial Temperature	CT	TOPER-CT	0°C	85°C	95°C
Industrial Temperature	IT	TOPER-IT	-40°C	85°C	95°C

NOTE:

1) The operating temperature is the case surface temperature on the center-top side of the DDR5 device. For measurements conditions, refer to JESD51-2 2) Normal is the maximum limit when device is operating in the Normal Temperature Mode
3) Extended is the maximum limit when device is operating in the Extended Temperature Mode
4) Support for the Industrial Temperature device is TBD

8.0 AC & DC INPUT MEASUREMENT LEVELS

8.1 CA Rx Voltage and Timings

The following draft assumes internal CA VREF. If the VREF is external, the specs will be modified accordingly.

The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA signals apply the same compliance mask and CS signal applies its own compliance mask independently. All signals applied to the compliance mask operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

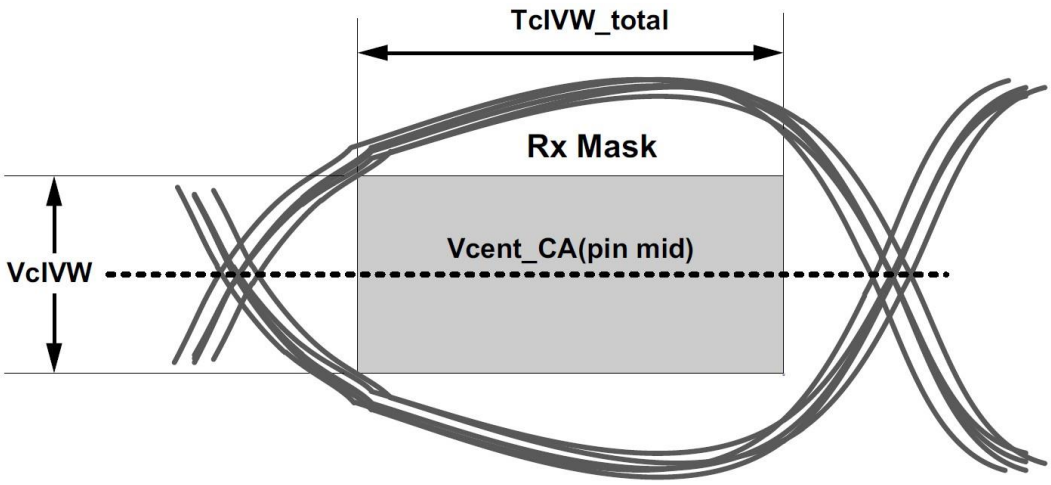


Figure 12. CA Receiver (Rx) mask

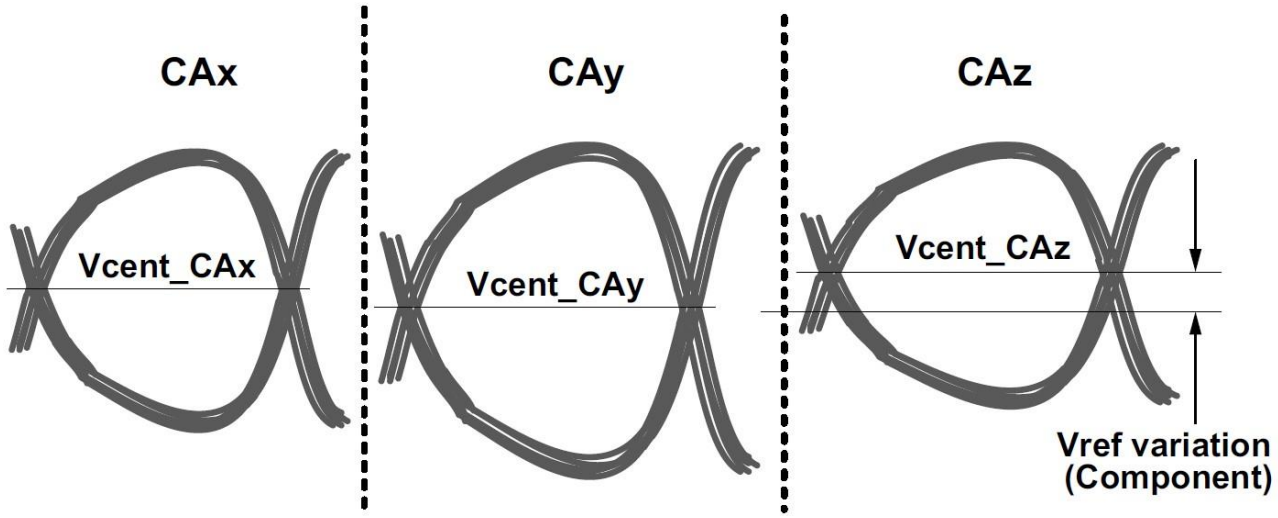
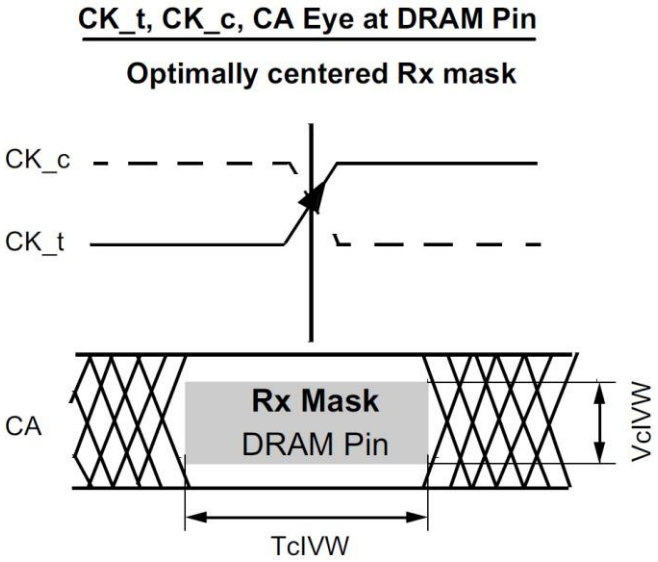


Figure 13. Across pin V_{REF}CA voltage variation

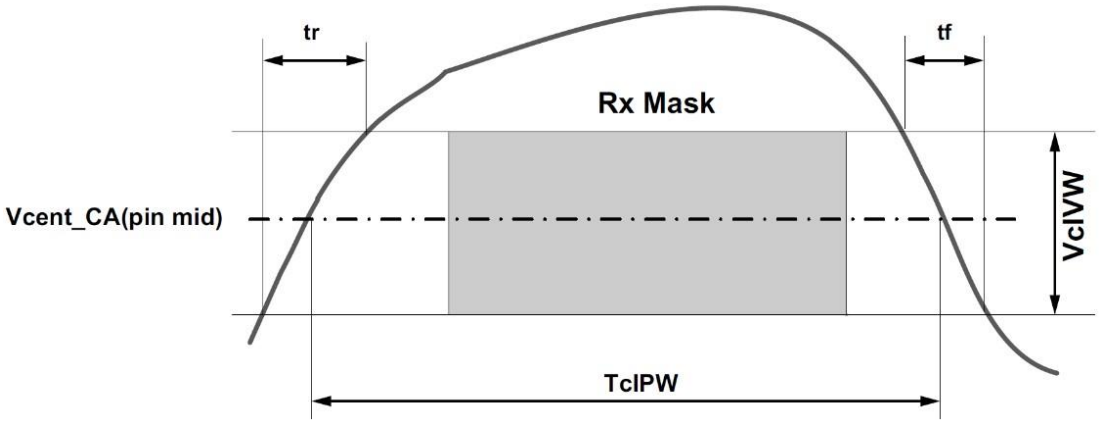
Vcent_CA(pin mid) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA Vcent level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 14. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level VREF will be set by the system to account for Ron and ODT settings.



TcIVW is not necessarily center aligned on CK_t/CK_c crossing at the DRAM pin, but is assumed to be center aligned at the DRAM Latch.

Figure 14. CA Timings at the DRAM Pins

All of the timing terms in Figure 14 are measured from the CK_t/CK_c to the center (midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around Vcent_CA (pin mid).



NOTE :
1) SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range

Figure 15. CA TcIPW and SRIN_cIVW definition (for each input pulse)

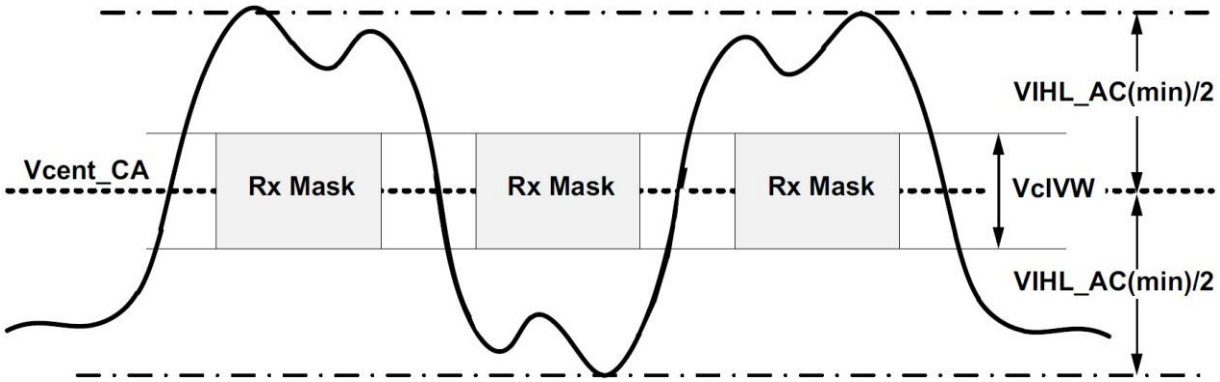


Figure 16. CA VIHL_AC definition (for each input pulse)

[Table 17] DRAM CA, CS Parametric values

Parameter	Symbol	DDR5-4400 to 4800		DDR5-5200 to 5600		Unit	Notes
		Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	-	130	-	80 (Cl max=0.55pF) 85 (Cl max=0.5pF)	mV	1,2,4
Rx Timing Window	TciVW	-	0.2	-	0.2	UI*	1,2,3,4,8
CA Input Pulse Amplitude	VIHL_AC	150		110		mV	7
CA Input Pulse Width	TciPW	0.58		0.58		UI*	5,8
Input Slew Rate over VcIVW	SRIN_cIVW	1	7	1	7	V/ns	6

NOTE:
1) CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift
2) Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid)
3) Rx differential CA to CK jitter total timing window at the VcIVW voltage levels
4) Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode
5) CA only minimum input pulse width defined at the Vcent_CA(pin mid)
6) Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid)
7) VIHL_AC does not have to be met when no transitions are occurring
8) UI=tCK(avg)min

8.2 Input Clock Jitter Specification

8.2.1 Overview

The clock is being driven to the DRAM either by the RCD for SODIMM modules. (Figure 17)

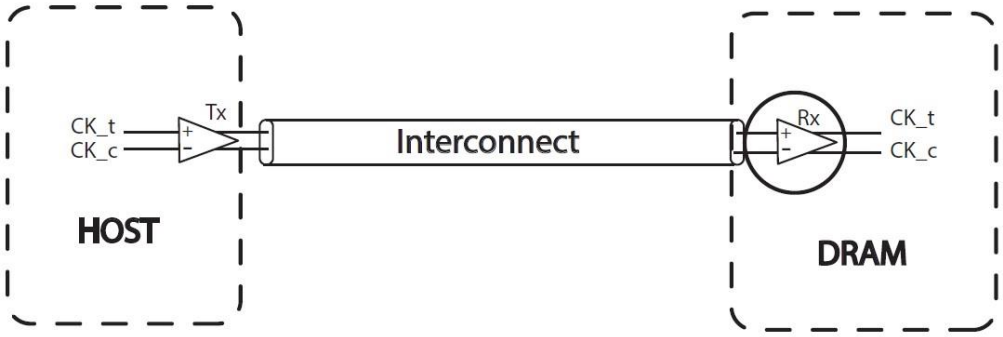


Figure 17. HOST driving clock signals to the DRAM

8.2.2 Specification for DRAM Input Clock Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. Input clock violating the min/max jitter values may result in malfunction of the DDR5 SDRAM device.

[Table 18] DRAM Input Clock Jitter Specifications

[BUJ=Bounded Uncorrelated Jitter; DCD=Duty Cycle Distortion; Dj=Deterministic Jitter; Rj=Random Jitter; Tj=Total jitter; pp=Peak-to-Peak]

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
DRAM Reference clock frequency	tCK	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	MHz	1,11
Duty Cycle Error	tCK_Duty_UI_Error	-	0.05	-	0.05	-	0.05	-	0.05	UI	1,4,11
Rj RMS value of 1-UI Jitter	tCK_1UI_Rj_NoBUJ	-	0.0037	-	0.0037	-	0.0037	-	0.0037	UI (RMS)	3,5,11
Dj pp value of 1-UI Jitter	tCK_1UI_Dj_NoBUJ	-	0.030	-	0.030	-	0.030	-	0.030	UI	3,6,11
Tj value of 1-UI Jitter	tCK_1UI_Tj_NoBUJ	-	0.090	-	0.090	-	0.090	-	0.090	UI	3,6,11
Rj RMS value of N-UI Jitter, where N=2,3	tCK_NUI_Rj_NoBUJ, where N=2,3	-	0.0040	-	0.0040	-	0.0040	-	0.0040	UI (RMS)	3,7,11
Dj pp value of N-UI Jitter, where N=2,3	tCK_NUI_Dj_NoBUJ, where N=2,3	-	0.074	-	0.074	-	0.074	-	0.074	UI	3,7,11
Tj value of N-UI Jitter, where N=2,3	tCK_NUI_Tj_NoBUJ, where N=2,3	-	0.140	-	0.140	-	0.140	-	0.140	UI	3,8,11
Rj RMS value of N-UI Jitter, where N=4,5,6,...,30	tCK_NUI_Rj_NoBUJ, where N=4,5,6,...,30	-	-	-	-	-	-	-	-	UI (RMS)	3,9,11,12
Dj pp value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Dj_NoBUJ, where N=4,5,6,...,30	-	-	-	-	-	-	-	-	UI	3,10,11,12
Tj value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Tj_NoBUJ, where N=4,5,6,...,30	-	-	-	-	-	-	-	-	UI	3,10,11,12

NOTE:

1) f0 = Data Rate/2, example: if data rate is 4800MT/s, then f0=2400
2) Rise and fall time slopes (V / nsec) are measured between +100 mV and -100 mV of the differential output of reference clock
3) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
4) Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI
5) Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD
6) Dj pp value of 1-UI jitter(after software assisted DCC).Without BUJ,but on-die system like noise present.Dj indicates Djdd of dual-Dirac fitting,after software correction of DCD
7) Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD
8) Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
9) Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD
10) Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD 11) The validation methodology for these parameters will be covered in future ballots
12) If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$

8.3 Differential Input Clock (CK_t, CK_c) Cross Point Voltage (VIX)

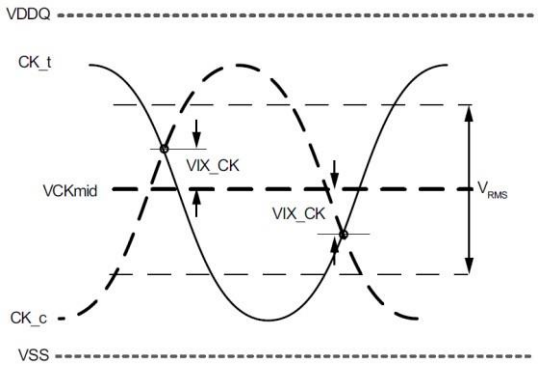


Figure 18. VIX Definition (CK)

[Table 19] Crosspoint Voltage (VIX) for Differential Input Clock

Parameter	Symbol	DDR5-4400 to 5600		Unit	Note
		min	max		
Clock differential input crosspoint voltage ratio	VIX_CK_Ratio	-	50	%	1,2,3

NOTE :
1) The VIX_CK voltage is referenced to VCKmid(mean) = (CK_t voltage + CK_c voltage) /2, where the mean is over 8 UI.
2) VIX_CK_Ratio = (|VIX_CK| / |VRMS|)*100%, where VRMS = RMS(CK_t voltage - CK_c voltage). 3) Only applies when both CK_t and CK_c are transitioning

8.4 Differential Input Clock Voltage Sensitivity

The differential input clock voltage sensitivity test provides the methodology for testing the receiver's sensitivity to clock by varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise. This specifies the Rx voltage sensitivity requirement. The system input swing to the DRAM must be larger than the DRAM Rx at the specified BER

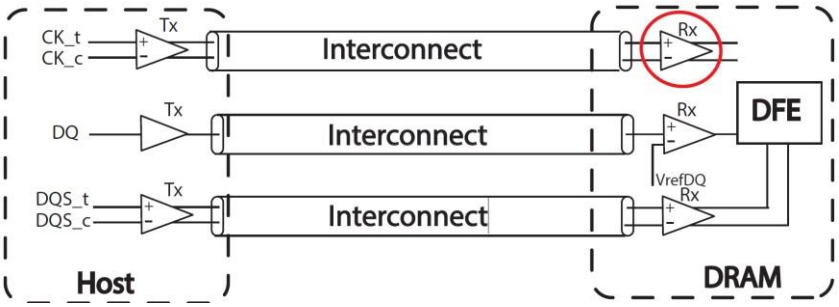


Figure 19. Example of DDR5 Memory Interconnect

8.4.1 Differential Input Clock Voltage Sensitivity Parameter

Differential input clock (CK_t, CK_c) VRx_CK is defined and measured as shown below. The clock receiver must pass the minimum BER requirements for DDR5.

[Table 20] Differential Input Clock Voltage Sensitivity Parameter

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Unit	Note
		min	max	min	max	min	max	min	max		
Input Clock Voltage Sensitivity (differential pp)	VRx_CK	-	180	-	160	-	140	-	120	mV	1,2

NOTE:
1) Refer to the minimum BER requirements for DDR5
2) The validation methodology for this parameter is TBD

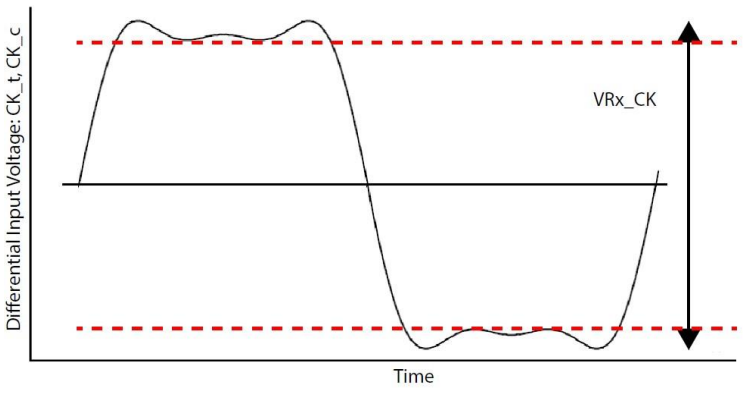


Figure 20. VRx_CK

8.4.2 Differential Input Voltage Levels for Clock

[Table 21] Differential Clock (CK_t, CK_c) Input Levels

From	Parameter	DDR5 4400 ~ 5600	Note
$V_{IHdiff}CK$	Differential input high measurement level (CK_t, CK_c)	0.75 x Vdiffpk-pk	1,2
$V_{ILdiff}CK$	Differential input low measurement level (CK_t, CK_c)	0.25 x Vdiffpk-pk	1,2

NOTE:
1) Vdiffpk-pk defined in Figure 21
2) Vdiffpk-pk is the mean high voltage minus the mean low voltage over TBD samples
3) All parameters are defined over the entire clock common mode range

8.4.3 Differential Input Slew Rate Definition for Clock (CK_t, CK_c)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown below.

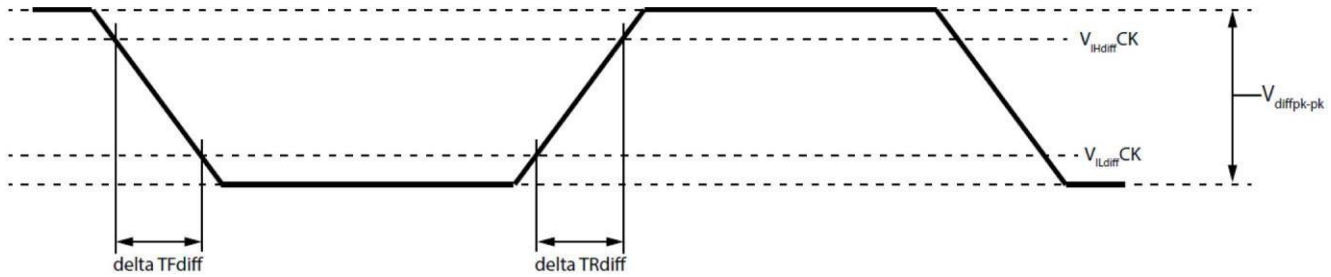


Figure 21. Differential Input Slew Rate Definition for CK_t, CK_c

[Table 22] Differential Input Slew Rate Definition for CK_t, CK_c

Parameter	Measured		Defined by	Notes
	From	To		
Differential Input slew rate for rising edge (CK_t - CK_c)	$VIL_{diff}CK$	$VIH_{diff}CK$	($VIH_{diff}CK$ - $VIL_{diff}CK$) /deltaTRdiff	
Differential Input slew rate for falling edge (CK_t - CK_c)	$VIH_{diff}CK$	$VIL_{diff}CK$	($VIH_{diff}CK$ - $VIL_{diff}CK$) /deltaTFdiff	

[Table 23] Differential Input Slew Rate for CK_t, CK_c

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Unit	Notes
		min	max	min	max	min	max	min	max		
Differential Input Slew Rate for CK_t, CK_c	SRIdiff_CK	2	14	2	14	2	30	2	30	V/ns	

8.5 Rx DQS Jitter Sensitivity

The receiver DQS jitter sensitivity test provides the methodology for testing the receiver's strobe sensitivity to an applied duty cycle distortion (DCD) and/ or random jitter (Rj) at the forwarded strobe input without adding jitter, noise and ISI to the data. The receiver must pass the appropriate BER rate when no cross-talk nor ISI is applied, and must pass through the combination of applied DCD and Rj.

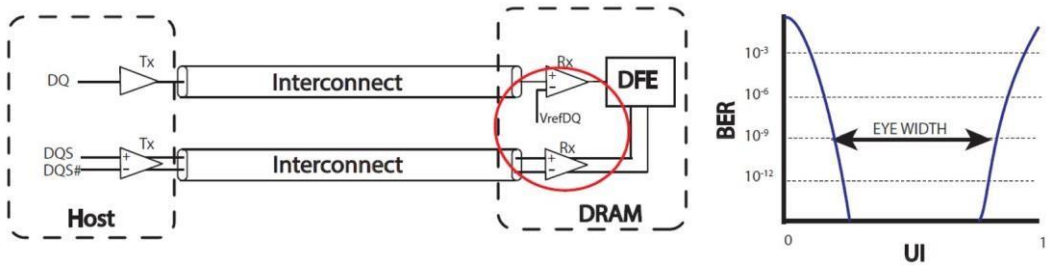


Figure 22. SDRAM's Rx Forwarded Strobes for Jitter Sensitivity Testing

8.5.1 Rx DQS Jitter Sensitivity Specification

The following table provides Rx DQS Jitter Sensitivity Specification for the DDR5 DRAM receivers when operating at various possible transfer rates. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

[Table 24] Rx DQS Jitter Sensitivity Specification

[BER = Bit Error Rate; DCD = Duty Cycle Distortion; Rj =Random Jitter]

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Unit	Notes
		min	max	min	max	min	max	min	max		
DQ Timing Width	tRx_DQ_tMargin	0.825	-	0.825	-	0.825	-	0.825	-	UI	1,2,3,8,9,10
Degradation of timing width compared to tRx_DQ_tMargin, with DCD injection in DQS	?tRx_DQ_tMargin _ DQS_DCD	-	0.06	-	0.06	-	0.06	-	0.06	UI	1,4,8,9,10
Degradation of timing width compared to tRx_DQ _tMargin, with Rj injection in DQS	?tRx_DQ_tMargin _ DQS_Rj	-	0.09	-	0.09	-	0.09	-	0.09	UI	1,5,8,9,10
Degradation of timing width compared to tRx_DQ_tMargin, with both DCD and Rj injection in DQS	?tRx_DQ_tMargin _ DQS_DCD_Rj	-	0.15	-	0.15	-	0.15	-	0.15	UI	1,2,6,8,9,10
Delay of any data lane relative to the DQS_t DQS_c crossing	tRx_DQS2DQ	114	738	114	729	114	721	114	714	ps	1,7,8,9,10
Delay of any data lane relative to any other data lane	tRX_DQ2DQ	-	50	-	50	-	50	-	50	ps	1,7,8,9,10 11,12

NOTE :

1) Validation methodology will be defined in future JEDEC ballots. 2UI is defined as 1tCK for this parameter.
2) Each of ?tRx_DQ_tMargin_DQS_DCD, ?tRx_DQ_tMargin_DQS_Rj, and ?tRx_DQ_tMargin_DQS _DCD_Rj can be relaxed by up to 5% if tRx_DQ_tMargin exceeds the spec by 5% or more.
3) DQ Timing Width - timing width for any data lane using repetitive patterns (check note 4 for the pattern) measured at BER=E-9.
4) Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to tRx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 "1s" and 3 "0s".

5) Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitude of Rj is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing
6) Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitudes of DCD and Rj are specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.
7) Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.
8) All measurements at BER=E-9.
9) This test should be done after the DQS and DQ Voltage Sensitivity tests are completed and passing.
10) The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.
11) DQ to DQ offset is skew between DQs within a nibble (x4) or a byte (x8, x16) at the DDR5 SDRAM balls.
12) This parameter is relative to the per-pin trained DQS2DQ value, and only appliesafterper-pin DQS2DQ training is complete.

8.5.2 Test Conditions for Rx DQS Jitter Sensitivity Tests

Table 25 lists the amount of Duty Cycle Distortion (DCD) and/or Random Jitter (Rj) that must be applied to the forwarded strobe when measuring the Rx DQS Jitter Sensitivity parameters specified in Table 24.

[Table 25] Test Conditions for Rx DQS Jitter Sensitivity Testing

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Applied DCD to the DQS	tRx_DQS_DCD	-	0.045	-	0.045	-	0.045	-	0.045	UI	1,2,3,6,7,10
Applied Rj RMS to the DQS	tRx_DQS_Rj	-	0.0075	-	0.0075	-	0.0075	-	0.0075	UI (RMS)	1,2,4,6,8,10
Applied DCD and Rj RMS to the DQS	tRx_DQS_DCD_Rj	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	UI	1,2,5,6,7,9,10

NOTE:
1) While imposing this spec, the strobe lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin.
The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.
2) The jitter response of the forwarded strobe channel will depend on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified, instead the response characterization done at the specified clock amplitude only. The specified voltages are at the Rx input pin
3) Various DCD values should be tested, complying within the maximum limits
4) Various Rj values should be tested, complying within the maximum limits
5) Various combinations of DCD and Rj should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of these injected jitter is specified in a separate table
6) Although DDR5 has bursty traffic, current available BERTs that can be used for this test do not support burst traffic patterns. A continuous strobe and continuous DQ are used for this parameter. The clock like pattern repeating 3 “1s” and 3 “0s” is used for this test.
7) Duty Cycle Distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI)
8) RMS value of Rj (specified as Edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)
9) Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)
10) The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification.
The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

8.6 Rx DQS Voltage Sensitivity

8.6.1 Overview

The receiver DQS (strobe) input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

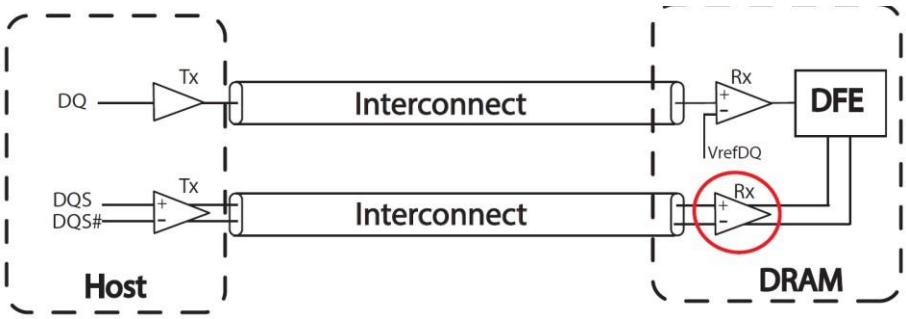


Figure 23. Example of DDR5 Memory Interconnect

8.6.2 Receiver DQS Voltage Sensitivity Parameter

Input differential (DQS_t, DQS_c) VRx_DQS is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

[Table 26] Rx DQS Input Voltage Sensitivity Parameter

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
DQS Rx Input Voltage Sensitivity (differential pp)	VRx_DQS	-	100	-	100	-	90	-	90	mV	1,2,3

NOTE:

1) Refer to the minimum BER requirements for DDR5
2) The validation methodology for this parameter is TBD
3) Test using clock like pattern of repeating 3 "1s" and 3 "0s"

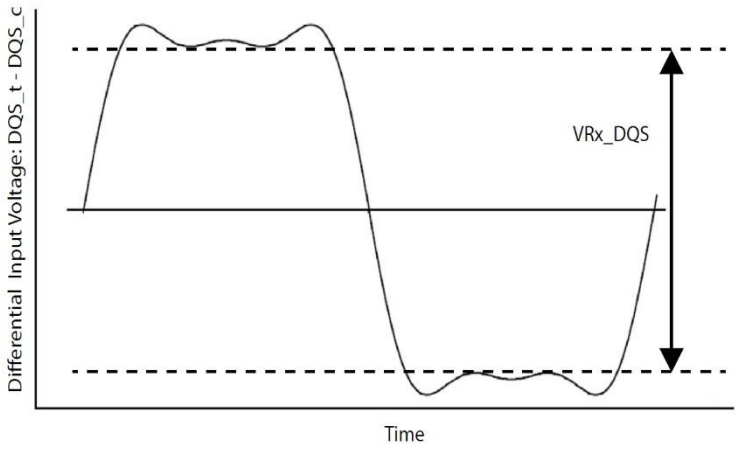


Figure 24. VRx_DQS

8.7 Differential Strobe (DQS_t, DQS_c) Input Cross Point Voltage (VIX)

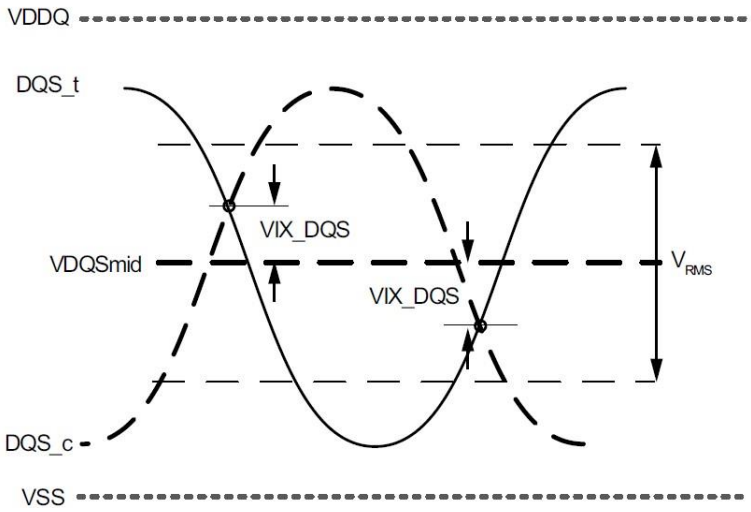


Figure 14. VIX Definition (DQS)

[Table 24] Crosspoint Voltage (VIX) for DQS Differential Input Signals

Parameter	Symbol	DDR5-4400 to 5600		Unit	Notes
		Min	Max		
DQS differential input crosspoint voltage ratio	VIX_DQS_Ratio	-	50	%	1,2,3

NOTE :
1) The VIX_DQS voltage is referenced to VDQSmid(mean) = (DQS_t voltage + DQS_c voltage) /2, where the mean is over 8 UI
2) VIX_DQS_Ratio = (|VIX_DQS| / |VRMS|)*100%, where VRMS = RMS(DQS_t voltage - DQS_c voltage)
3) Only applies when both DQS_t and DQS_c are transitioning (including preamble)

8.8 Rx DQ Voltage Sensitivity

8.8.1 Overview

The receiver data input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

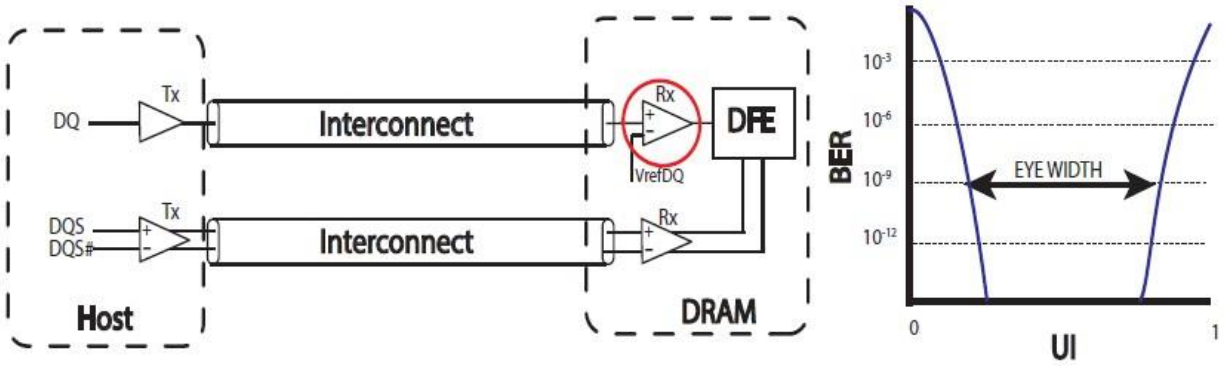


Figure 15. Example of DDR5 Memory Interconnect

8.8.2 Receiver DQ Input Voltage Sensitivity Parameters

Input single-ended VRx_DQ is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

[Table 20] Rx DQ Input Voltage Sensitivity Parameters

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Minimum DQ Rx input voltage sensitivity applied around Vref	VRx_DQ	-	65	-	65	-	60	-	60	mV	1,2,3

NOTE :
1) Refer to the minimum BER requirements for DDR5
2) The validation methodology for this parameter is TBD
3) Recommend testing using clock like pattern such as repeating 3 "1s" and 3 "0s"

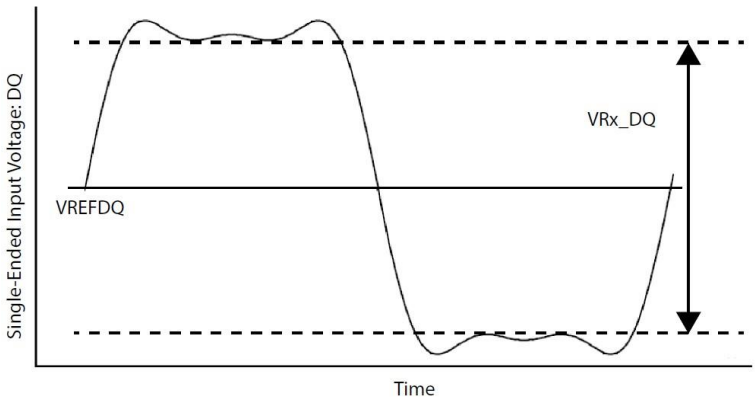


Figure 16. VRx_DQ

8.8.3 Differential Input Levels for DQS

[Table 21] Differential Input Levels for DQS (DQS_t, DQS_c)

From	Parameter	DDR5 4400 to 5600	Notes
$V_{IHdiff}DQS$	Differential input high measurement level (DQS_t, DQS_c)	0.75 x $V_{diffpk-pk}$	1,2,3
$V_{ILdiff}DQS$	Differential input low measurement level (DQS_t, DQS_c)	0.25 x $V_{diffpk-pk}$	1,2,3

NOTE :
1) Vdiffpk-pk defined in Figure 17
2) Vdiffpk-pk is the mean high voltage minus the mean low voltage over TBD samples
3) All parameters are defined over the entire clock common mode range

8.8.4 Differential Input Slew Rate for DQS_t, DQS_c

Input slew rate for differential signals are defined and measured as shown below.

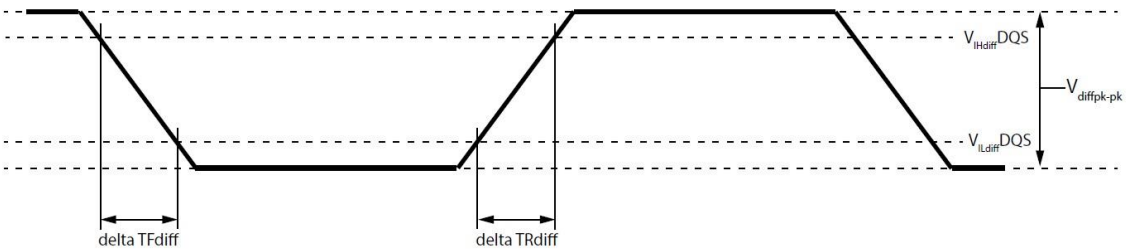


Figure 17. Differential Input Slew Rate Definition for DQS_t, DQS_c

[Table 22] Differential Input Slew Rate Definition for DQS_t, DQS_c

Parameter	Measured		Defined by	Notes
	From	To		
Differential Input slew rate for rising edge (DQS_t, DQS_c)	$V_{ILdiff}DQS$	$V_{IHdiff}DQS$	($V_{IHdiff}DQS$ - $V_{ILdiff}DQS$) / deltaTRdiff	
Differential Input slew rate for falling edge (DQS_t, DQS_c)	$V_{IHdiff}DQS$	$V_{ILdiff}DQS$	($V_{IHdiff}DQS$ - $V_{ILdiff}DQS$) / deltaTFdiff	

[Table 23] Differential Input Slew Rate for DQS_t, DQS_c

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for DQS_t, DQS_c	SRIdiff_DQS	1.5	30	1.5	30	2.0	30	2.0	30	Vins	1

NOTE :
1) Only applies when both DQS_t and DQS_c are transitioning.

8.9 Rx Stressed Eye

The stressed eye tests provide the methodology for creating the appropriate stress for the DRAM's receiver with the combination of ISI (both loss and reflective), jitter (Rj, Dj, DCD), and crosstalk noise. The receiver must pass the appropriate BER rate when the equivalent stressed eye is applied through the combination of ISI, jitter and crosstalk

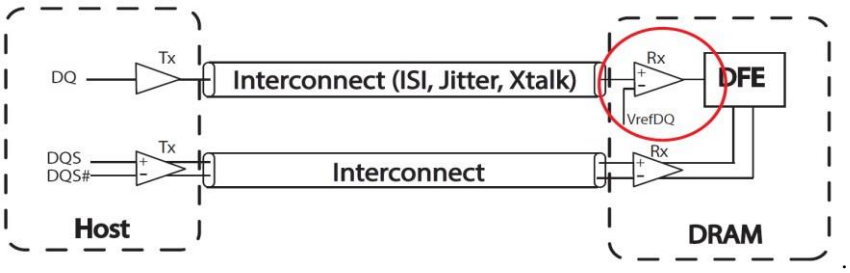


Figure 18. Example of Rx Stressed Test Setup in the Presence of ISI, Jitter and Crosstalk

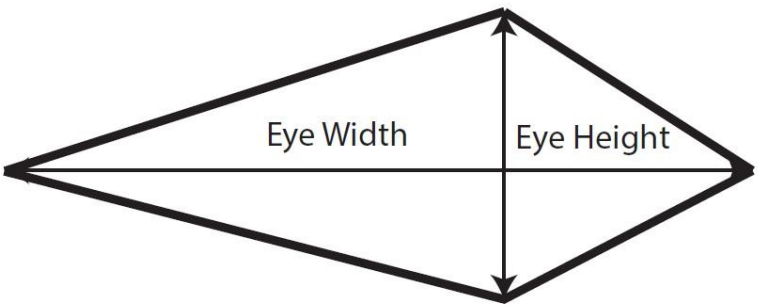


Figure 19. Example of Rx Stressed Eye Height and Eye Width

8.9.1 Parameters for DDR5 Rx Stressed Eye Tests

[Table 24] Test Conditions for Rx Stressed Eye Tests

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Eye height of stressed eye for Golden Reference Channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	-	75	-	70	-	65	-	60	mV	1,2,3,4,5,6,7,8,9
Eye width of stressed eye Golden Reference Channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	-	0.25	-	0.25	-	0.235	-	0.235	UI	1,2,3,4,5,6,7,8,9
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	600	-	600	-	600	-	600	mV	1,2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	0	0.45	0	0.45	0	0.45	0	0.45	UI p-p	1,2
Injected Random wide band (10 MHz-1 GHz) Jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	0	0.04	0	0.04	0	0.04	0	0.04	UI RMS	1,2
Injected voltage noise as PRBS23, or Injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	0	125	0	125	0	125	0	125	mV p-p	1,2
Golden Reference Channel 1 Characteristics as measured at TBD	Golden_Ref_Channel_1_Characteristics									dB	3

NOTE :

1) Must meet minimum BER of $1E^{-16}$ or better requirement with the stressed eye at the slice of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER E^{-9} and extrapolating to BER E^{-16}.
2) These parameters are applied on the defined golden reference channel with parameters TBD.
1) DFE Tap 1-4 Bias settings that give the best eye margin are used and referring to Table 132, Min/Max Ranges for the DFE Tap Coefficients. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 shall be less than 60mV (|Tap-2| + |Tap-3| + |Tap-4| < 60mV) after the tap multiflier is applied.
2) Evaluated with no DC supply voltage drift.
3) Evaluated with no temperature drift.
4) Supply voltage noise limited according to DC bandwidth spec, see DC Operating Conditions
5) The stressed eye is to be assumed to have a diamond shape
6) The VREFDQ, DFE Gain Bias Step, and DFE Taps 1,2,3,4 Bias Step can be adjusted as needed, without exceeding the specifications, for this test, including the limits placed in Note 3.
7) The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, VrefDQ, and DFE solution to give the best eye margin.
10) The Rx stressed eye spec applies at 2933MT/s and faster data rates.
11) EH/EW are measured at the slicer of the receiver

8.10 Connectivity Test Mode - Input level and Timing Requirement

During CT Mode, input levels are defined below.
TEN pin: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ
CS_n: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.
Test Input pins: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.
RESET_n: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

Upon the assertion of the TEN pin, the CK_t and CK_c signals will be ignored and the DDR5 memory device will enter into the CT mode after time tCT_Enable. In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

The TEN pin may be asserted after the DRAM has completed power-on, after RESET_n has de-asserted, the wait time after the RESET_n de-assertion has elapsed, and prior to starting clocks (CK_t, CK_c).

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR5 memory device are unknown and the integrity of the original content of the memory array is not guaranteed; therefore, the reset initialization sequence is required.

All output signals at the test output pins will be stable within tCT_valid after the test inputs have been applied to the test input pins with TEN input and CS_n input maintained High and Low respectively.

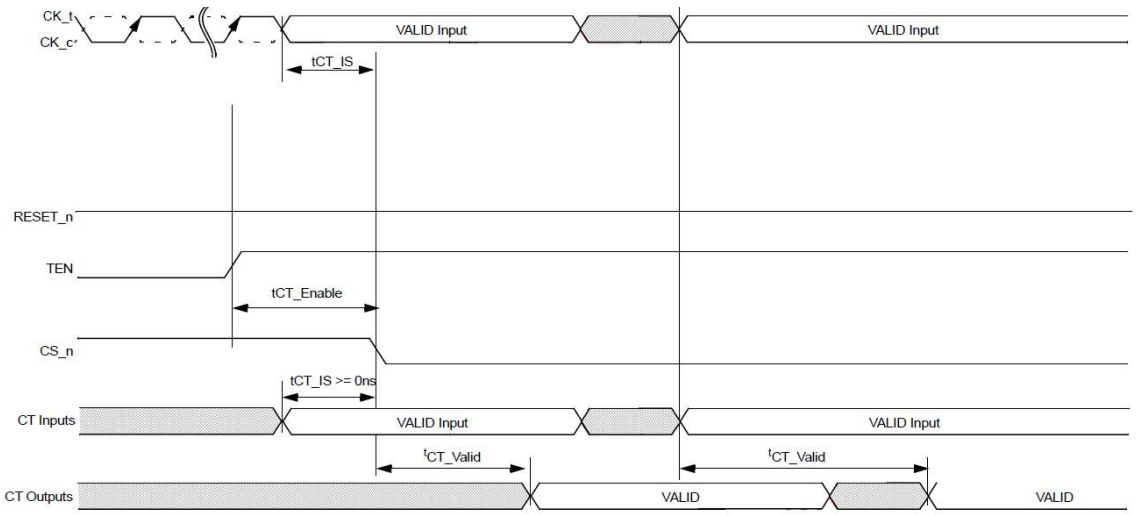


Figure 20. Timing Diagram for Connectivity Test (CT) Mode

[Table 25] AC parameters for Connectivity Test (CT) Mode

Symbol	Min	Max	Unit
tCT_IS	0	-	ns
tCT_Enable	200	-	ns
tCT_Valid	-	200	ns

8.10.1 Connectivity Test (CT) Mode Input Levels

Following input parameters will be applied for DDR5 SDRAM Input Signals during Connectivity Test Mode.

[Table 26] CMOS rail to rail Input Levels for TEN, CS_n and Test inputs

Parameter	Symbol	Min	Max	Unit	Notes
TEN AC Input High Voltage	VIH(AC)_TEN	0.8 * VDDQ	VDDQ	V	1
TEN DC Input High Voltage	VIH(DC)_TEN	0.7 * VDDQ	VDDQ	V	
TEN DC Input Low Voltage	VIL(DC)_TEN	VSS	0.3 * VDDQ	V	
TEN AC Input Low Voltage	VIL(AC)_TEN	VSS	0.2 * VDDQ	V	2
TEN Input signal Falling time	TF_input_TEN	-	10	ns	
TEN Input signal Rising time	TR_input_TEN	-	10	ns	

NOTE :
1) Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
2) Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

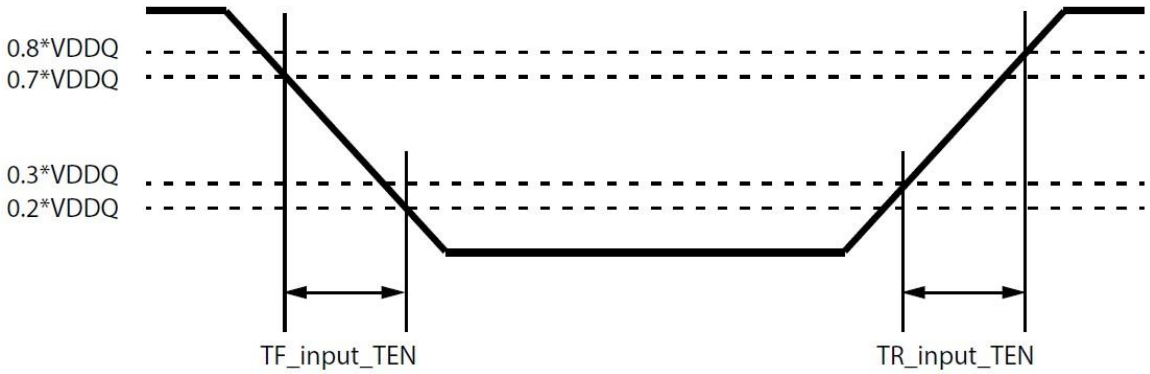


Figure 21. TEN Input Slew Rate Definition

8.10.2 CMOS rail to rail Input Levels for RESET_n

[Table 27] CMOS rail to rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDDQ	VDDQ	V	5
DC Input High Voltage	VIH(DC)_RESET	0.7*VDDQ	VDDQ	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDDQ	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDDQ	V	6
Rising time	TR_RESET	-	1.0	us	
RESET pulse width	tPW_RESET	1.0	-	us	3,4

NOTE :
1) After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
2) Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3) RESET is destructive to data contents.

4) This definition is applied only for “Reset Procedure at Power Stable”.
5) Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
6) Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

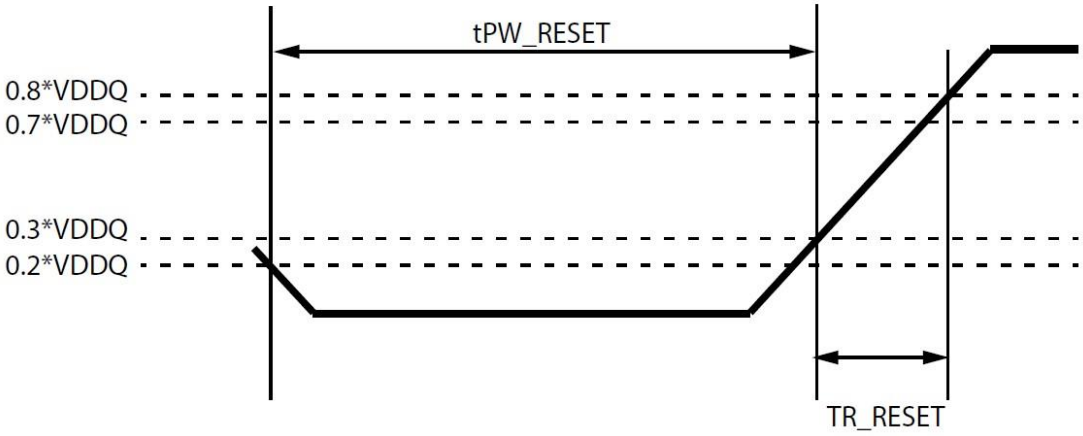


Figure 22. RESET_n Input Slew Rate Definition

9.0 AC&DC OUTPUT MEASUREMENT LEVELS and TIMING

9.1 Output Driver DC Electrical Characteristics for DQS and DQ

The DDR5 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in the figure below.

Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$ under the condition that RON_{Pu} is off

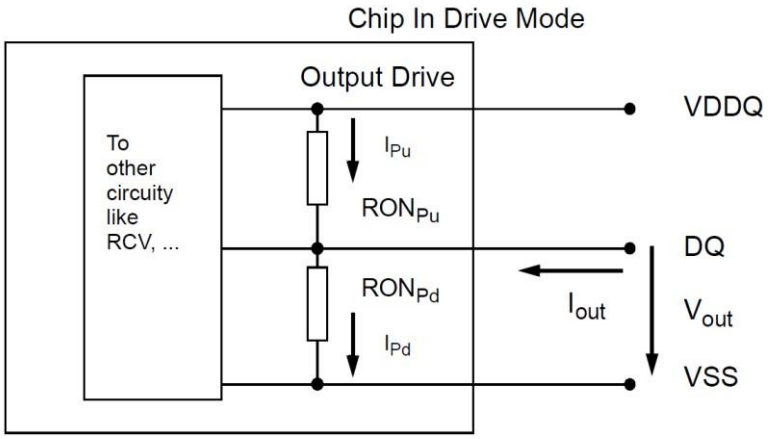


Figure 34. Output Driver Impedance Ron

[Table 36] Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm; entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ			10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ			10	%	1,2,4

NOTE :

1) The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD)"ZQ Calibration Commands" section.
2) Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.
3) Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately;

Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4) RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

5) This parameter of x16 device is specified for Upper byte and Lower byte.

9.2 Output Driver DC Electrical Characteristics for Loopback Signals LBDQS, LBDQ

The DDR5 Loopback driver supports 34 ohms. A functional representation of the output buffer is shown in the figure below.

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\,out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\,out|}$$ under the condition that RON_{Pu} is off

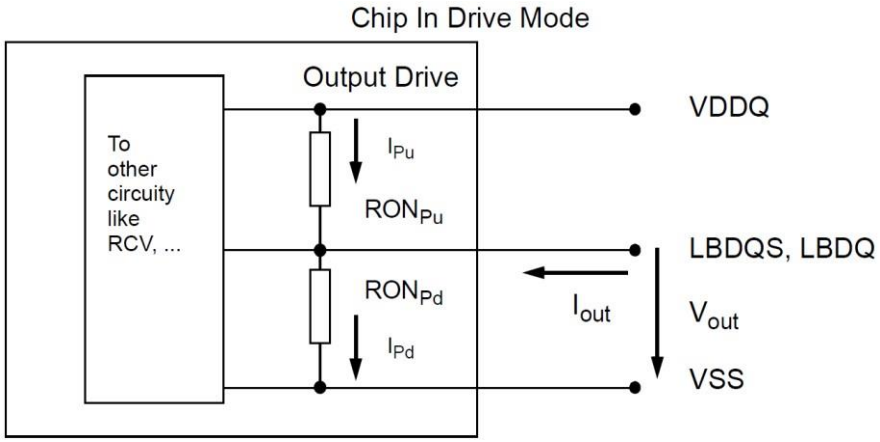


Figure 35. Output Driver for Loopback Signals

[Table 37] Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1,2
Mismatch between pull-up and pull- down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1,2,3,4
Mismatch LBDQS-LBDQ within device variation pull-up, MMPudd		VOMdc= 0.8* VDDQ			10	%	1,2,4
Mismatch LBDQS-LBDQ within device variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ			10	%	1,2,4

NOTE :

1) The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD)"ZQ Calibration Commands" section.
2) Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.
3) Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately;

Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4) RON variance range ratio to RON Nominal value in a given component, including LBDQS and LBDQ

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

9.3 Loopback Output Timing

Loopback strobe LBDQS to Loopback data LBDQ relationship is illustrated inFigure 36.

- tLBQSH describes the single-ended LBDQS strobe high pulse width
- tLBQSL describes the single-ended LBDQS strobe low pulse width
- tLBDQSQ describes the latest valid transition of LBDQ measured at both rising and falling edges of LBDQS
- tLBQH describes the earliest invalid transition of LBDQ measured at both rising and falling edges of LBDQS
- tLBDVW describes the data valid window per device per UI and is derived from (tLBQH-tLBDQSQ) of each UI on a given DRAM

[Table 38] Loopback Output Timing Parameters

Speed		DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Units	Notes
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Loopback LBDQS Output Low Time	tLBQSL	0.7	-	0.7	-	0.7	-	0.7	-	tCK	1
Loopback LBDQS Output High Time	tLBQSH	0.7	-	0.7	-	0.7	-	0.7	-	tCK	1
Loopback LBDQS to LBDQ Skew	tLBDQSQ	0.5	-	0.5	-	0.5	-	0.5	-	tCK/2	1,2
Loopback LBDQ Output Time from LBDQS	tLBQH	0.5	-	0.5	-	0.5	-	0.5	-	tCK/2	1,2
Loopback Data valid window (tLBQH-tLBDQSQ) of each UI per DRAM	tLBDVW	1.6	-	1.6	-	1.6	-	1.6	-	tCK/2	1

NOTE:

1) Based on Loopback 4-way interleave setting.
2) tLBQ_Set is measured from LBDQ first transition to LBDQS falling edge and tLBQ_Hld is measured from LBDQS falling edge to LBDQ last transition.

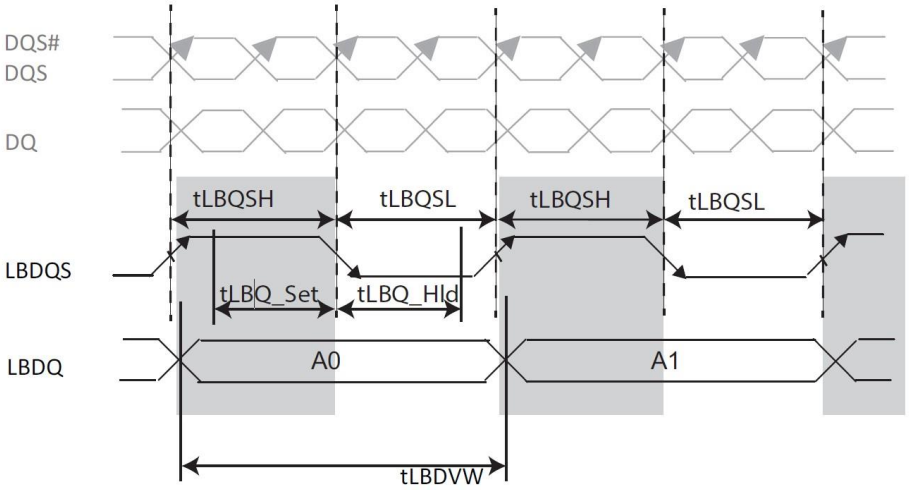


Figure 36. Loopback Strobe to Data Relationship

9.3.1 Alert_n output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|\ Iout\ |} \quad \text{under the condition that } RON_{Pu} \text{ is off}$$

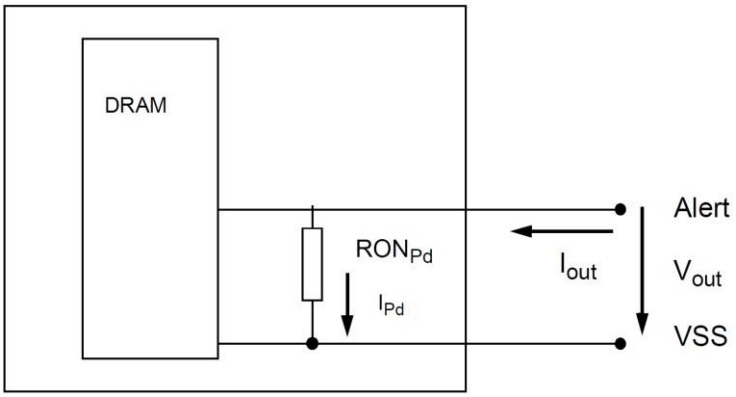


Figure 37. Alert Driver

Resistor	Vout	Min	Max	Unit	Notes
RON_{Pd}	VOLdc= 0.1* VDDQ	0.3	1.1	$R_{ZQ}/7$	
	V_{OMdc} = 0.8* VDDQ	0.4	1.1	$R_{ZQ}/7$	
	V_{OHdc} = 0.95* VDDQ	0.4	1.25	$R_{ZQ}/7$	

9.3.2 Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied to the Test Output Pin during Connectivity Test (CT) Mode. The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ}-V_{OUT}}{|\ Iout\ |}$$

$$RON_{Pd\_CT} = \frac{V_{OUT}}{|\ Iout\ |}$$

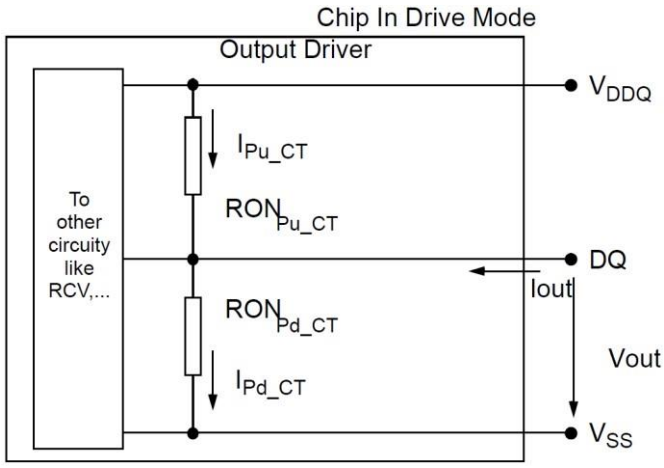


Figure 38. Output Driver

RONNOM_CT	Resistor	Vout	Max	Units	NOTE
34Ω	RONPd_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1,2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1,2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1,2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1,2
	RONPu_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1,2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1,2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1,2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1,2

NOTE:
1) Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined 2) Uncalibrated drive strength tolerance is specified at +/- 30%

9.4 Single-ended Output Levels - VOL/VOH

[Table 39] Single-ended Output levels

Symbol	Parameter	DDR5-4400 to 5600	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x $V_{pk\text{-}pk}$	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x $V_{pk\text{-}pk}$	V	1

NOTE:

1) $V_{pk\text{-}pk}$ is the mean high voltage minus the mean low voltage over 8UI samples

9.5 Single-Ended Output Levels - VOL/VOH for Loopback Signals

[Table 40] Single-ended Output levels for Loopback Signals

Symbol	Parameter	DDR5-4400 to 5600	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x $V_{pk\text{-}pk}$	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x $V_{pk\text{-}pk}$	V	1

NOTE:
1) $V_{pk\text{-}pk}$ is the mean high voltage minus the mean low voltage over 8UI samples

9.6 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL} and V_{OH} for single ended signals as shown in Table 41 and Figure 39.

[Table 41] Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}	V_{OH}	[V_{OH}-V_{OL}] / delta TRse
Single ended output slew rate for falling edge	V_{OH}	V_{OL}	[V_{OH}-V_{OL}] / delta TFse

NOTE:
1) Output slew rate is verified by design and characterization, and may not be subject to production test

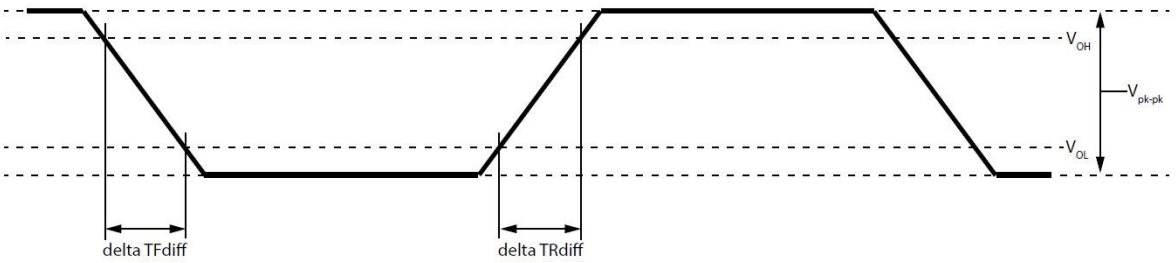


Figure 39. Single-ended Output Slew Rate Definition

[Table 42] Single-ended Output Slew Rate

Speed		DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Units	Notes
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Single ended output slew rate	SRQse	8	24	8	24	12	24	12	24	V/ns	

9.7 Differential Output Levels

[Table 43] Differential Output levels

Symbol	Parameter	DDR5-4400 to 5600	Units	Notes
V_{OHdiff}	Differential output high measurement level (for output SR)	0.75 x $V_{diffpk-pk}$	V	1
V_{OLdiff}	Differential output low measurement level (for output SR)	0.25 x $V_{diffpk-pk}$	V	1

NOTE:

1) $V_{diffpk-pk}$is the mean high voltage minus the mean low voltage over 8UI samples

9.8 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OLdiff} and V_{OHdiff} for differential signals as shown in Table 44 and Figure 40.

[Table 44] Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{OLdiff}	V_{OHdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}	V_{OLdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TFdiff

NOTE:

1) Output slew rate is verified by design and characterization, and may not be subject to production test

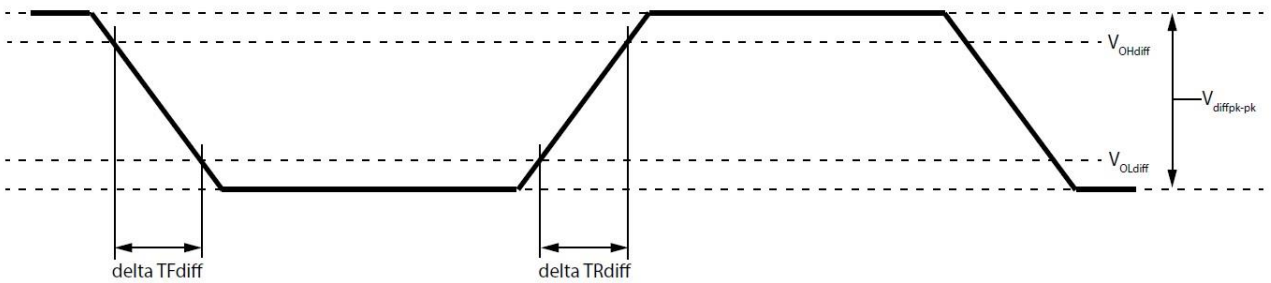


Figure 40. Differential Output Slew Rate Definition

[Table 45] Differential Output Slew Rate

Speed		DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Units	Notes
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Differential output slew rate	SRQdiff	16	48	16	48	24	48	24	48	V/ns	

9.9 Tx DQS Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in Table 46.

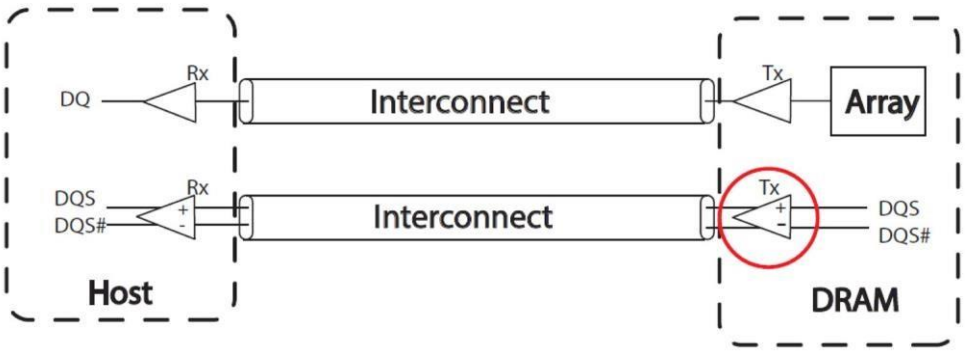


Figure 41. Tx DQS Jitter

9.9.1 Tx DQS Jitter Parameters

[Table 46] Tx DQS Jitter Parameters

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Rj RMS Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1,2,3,4, 5,6,7,8,9, 10,11,12
Dj pp Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Dj_NoBUJ	-	0.150	-	0.150	-	0.130	-	0.130	UI	1,2,3,5,6, 7,8,9,10,11
Rj RMS Value of N-UI jitter without BUJ, where 1<N< 4	tTx_DQS_NUI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1,2,3,5,6, 7,8,9,10,11 12
Dj pp Value of N-UI Jitter without BUJ, where 1<N < 4	tTx_DQS_NUI_Dj_NoBUJ	-	0.150	-	0.150	-	0.130	-	0.130	UI	1,2,3,5,6, 7,8,9,10,11

NOTE:

1) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all thetransmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
2) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter

lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers, so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility

3) The validation methodology for these parameters will be covered in future ballots
4) Rj RMS value of 1-UI jitter. Without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD
5) See Chapter 12 for details on the minimum BER requirements
6) See Chapter 12 for details on UI, NUI and Jitter definitions
7) Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running the Tx DQ Jitter test
8) The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44, and the Mode Registers for the Per Pin DCA of DQS are MR103 - MR110
9) Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test
10) These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to “1” to enable this feature
11) Tested on the CTC2 card only
12) The max value of tTx_DQS_Rj_1UI_NoBUJ and tTx_DQS_Rj_NUI_NoBUJ can be 6mUI RMS

9.10 Tx DQ Jitter

9.10.1 Overview

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in Table 47.

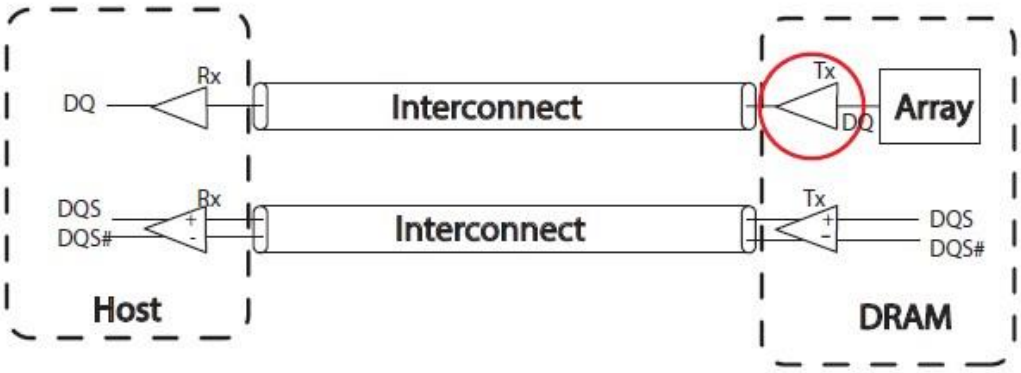


Figure 42. Tx DQ Jitter

9.10.2 Tx DQ Jitter Parameters

[Table 47] Tx DQ Jitter Parameters

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-4400 to 4800		DDR5-5200 to 5600		Unit	Notes
		Min	Max	Min	Max		
Rj RMS Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Rj _NoBUJ	-	tCK_1UI_Rj_ NoBUJ+0.002	-	tCK_1UI_Rj_ NoBUJ+0.002	UI (RMS)	1,2,3,4, 5,6,7,8,9, 10,11,12
Dj pp Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Dj _NoBUJ	-	0.150	-	0.130	UI	1,2,3,5,6, 7,8,9,10,11
Rj RMS Value of N-UI jitter without BUJ, where 1<N< 4	tTx_DQS_NUI_Rj _NoBUJ	-	tCK_NUI_Rj_ NoBUJ+0.002	-	tCK_NUI_Rj_ NoBUJ+0.002	UI (RMS)	1,2,3,5,6, 7,8,9,10,11 12
Dj pp Value of N-UI Jitter without BUJ, where 1<N < 4	tTx_DQS_NUI_Dj _NoBUJ	-	0.160	-	0.130	UI	1,2,3,5,6, 7,8,9,10,11
Delay of any data lane relative to strobe lane	tTx_DQS2DQ	-0.100	0.100	-0.100	0.100		

NOTE:

1) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmittermeasurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all thetransmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant.To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
2) On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
3) The validation methodology for these parameters will be covered in future ballots
4) Rj RMS value of 1-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD 5) Delay of any data lane relative to strobe lane, as measured at Tx output
6) Vref noise level to DQ jitter should be adjusted to minimize DCD
7) See Chapter 12 for details on the minimum BER requirements
8) See Chapter 12 for details on UI, NUI and Jitter definitions
9) Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test
10) The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where 0≤x≤7, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where 0≤y≤7. 11) Spread Spectrum Clocking (SSC) must be disabled while running this test
12) These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to “1” to enable this feature.
13) Tested on the CTC2 card only
14) The max value of tTx_DQ_Rj_1UI_NoBUJ and tTx_DQ_Rj_NUI_NoBUJ can be 6mUI RMS

9.11 Tx DQ Stressed Eye

Tx DQ stressed eye height and eye width must meet minimum specification values at BER=E^{-9} and confidence level 99.5%. Tx DQ Stressed Eye shows the DQS to DQ skew for both Eye Width and Eye Height. In order to support different Host Receiver (Rx) designs, it is the responsibility of the Host to insure the advanced DQS edges are adjusted accordingly via the Read DQS Offset Timing mode register settings (MR40 OP[3:0]).

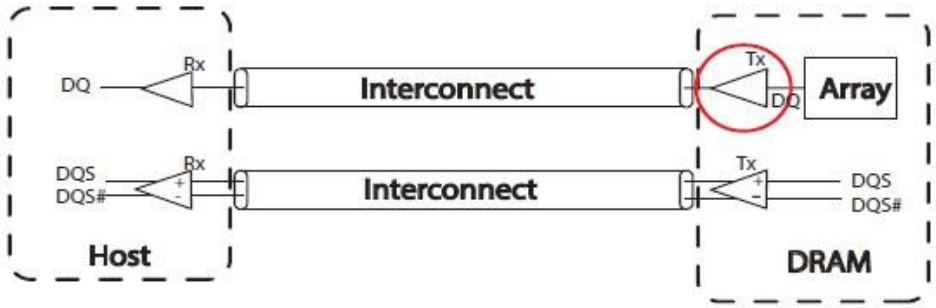


Figure 43. Example of DDR5 Memory Interconnect

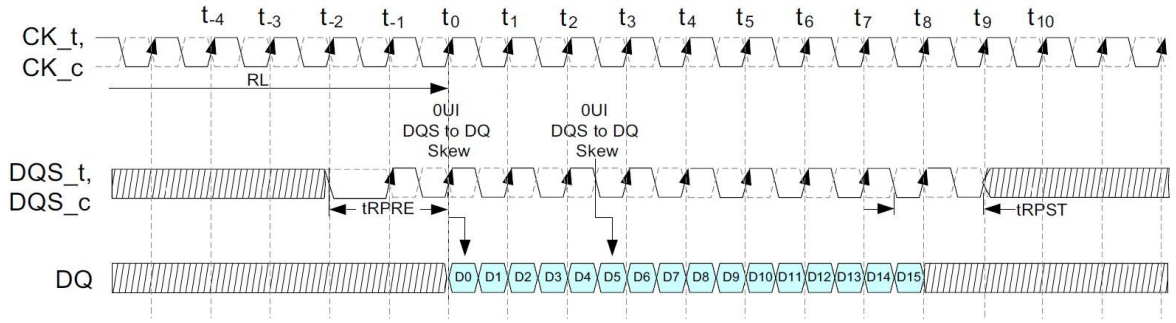


Figure 44. Read burst example for pin DQx depicting bit 0 and 5 relative to the DQS edge for 0 UI skew

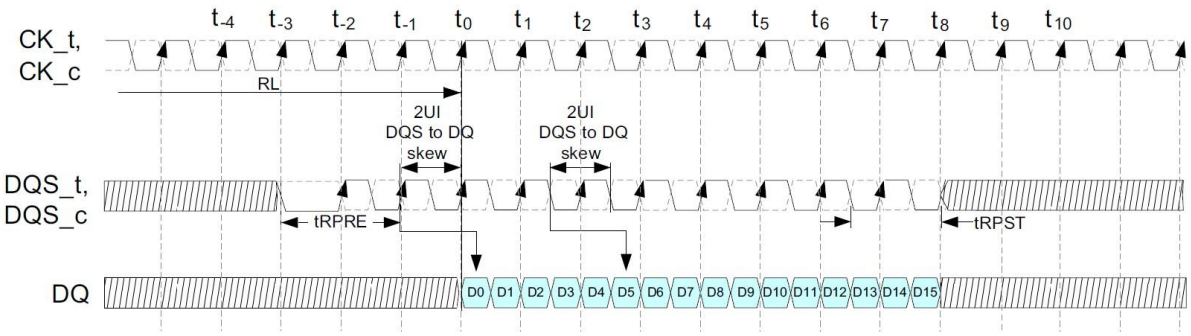


Figure 45. Read burst example for pin DQx depicting bit 0 and 5 relative to the DQS edge for 2 UI skew with Read DQS Offset Timing set to 1 Clock (2UI)

9.11.1 Tx DQ Stressed Eye Parameters

[Table 48] Tx DQ Stressed Eye Parameters

[EH=Eye Height, EW=Eye Width; BER=Bit Error Rate, SES=Stressed Eye Skew]

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Eye Width specified at the transmitter with a skew between DQ and DQS of 1UI	TxEW_DQ_SES_1UI	0.72	-	0.72	-	0.74	-	0.74	-	UI	1,2,3,4,6,7, 8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 2UI	TxEW_DQ_SES_2UI	0.72	-	0.72	-	0.74	-	0.74	-	UI	1,2,3,4,6,7, 8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 3UI	TxEW_DQ_SES_3UI	0.72	-	0.72	-	0.74	-	0.74	-	UI	1,2,3,4,6,7, 8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 4UI	TxEW_DQ_SES_4UI	-	-	-	-	0.74	-	0.74	-	UI	1,2,3,4,6,7, 8,9,10

NOTE:

1) Minimum BER E-9 and Confidence Level of 99.5% per pin
2) Refer to the minimum Bit Error Rate (BER) requirements for DDR5
3) The validation methodology for these parameters is TBD
4) Mismatch is defined as DQS to DQ mismatch, in UI increments
5) The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable
6) Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test
7) The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQS are MR103-MR110, the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where 0≤x≤7, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where 0≤y≤7.
8) Spread Spectrum Clocking (SSC) must be disabled while running this test
9) These parameters are tested using the continuous PRBS8 LFSR training pattern which are sent out on all DQ lanes off the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.
10) Tested on the CTC2 card only
11) Matched DQS to DQ would require the DQs to be adjusted by 0.5UI to place it in the center of the DQ eye. 1UI mismatch would require the DQS to be adjusted 1.5UI. Generally, for XUI mismatch the DQ must be adjusted XUI + 0.5UI to be placed in the center of the eye

10.0 SPEED BIN

[Table 49] DDR5-4400 Speed Bins and Operations

Speed Bin					DDR5-4400		Unit	Notes
CL-nRCD-nRP					36-36-36			
Parameter				Symbol	min	max		
Read command to first data				tAA	16.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	16.000	-	ns	7
Row Precharge Time				tRP	16.000	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	48.000	-	ns	7,8
CAS Write Latency				CWL	RESERVED		nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRP-min (ns)[5]	Read CL[12]	Supported Frequency Down Bins				
-	20.952	-	22	tCK(AVG)	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	ns	
3200AN	15.000	15.000	24	tCK(AVG)	RESERVED		ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	ns	
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED		ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED		ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	ns	
4400AN	14.545	14.545	32	tCK(AVG)	RESERVED		ns	
Supported CL					22,26,28,30,32,36,40		nCK	12

[Table 50] DDR5 4800 Speed Bins and Operations

Speed Bin					DDR5-4800		Unit	Notes
CL-nRCD-nRP					40-39-39			
Parameter				Symbol	min	max		
Read command to first data				tAA	16.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	16.000	-	ns	7
Row Precharge Time				tRP	16.000	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	48.000	-	ns	7,8
CAS Write Latency				CWL			nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRP-min (ns)[5]	Read CL[12]	Supported Frequency Down Bins				
-	20.952	-	22	tCK(AVG)	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	ns	
3200AN	15.000	15.000	24	tCK(AVG)	RESERVED		ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	ns	
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED		ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED		ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	ns	
4400AN	14.545	14.545	32	tCK(AVG)	RESERVED		ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	ns	
4800AN	14.166	14.166	34	tCK(AVG)	RESERVED		ns	
Supported CL					22,26,28,30,32,36, 40,42		nCK	12

[Table 51] DDR5 5200 Speed Bins and Operations

Speed Bin					DDR5-5200		Unit	Notes
CL-nRCD-nRP					42-42-42			
Parameter				Symbol	min	max		
Read command to first data				tAA	16.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	16.000	-	ns	7
Row Precharge Time				tRP	16.000	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	48.000	-	ns	7,8
CAS Write Latency				CWL			nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRP-min (ns)[5]	Read CL[12]	Supported Frequency Down Bins				
-	20.952	-	22	tCK(AVG)	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	ns	
3200AN	15.000	15.000	24	tCK(AVG)	RESERVED		ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	ns	
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED		ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED		ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	ns	
4400AN	14.545	14.545	32	tCK(AVG)	RESERVED		ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	ns	
4800AN	14.166	14.166	34	tCK(AVG)	RESERVED		ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416		
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416		
5200AN	14.615	14.615	38	tCK(AVG)	RESERVED			
Supported CL					22,26,28,30,32,36, 40,42,46		nCK	12

[Table 52] DDR5 5600 Speed Bins and Operations

Speed Bin					DDR5-5600		Unit	Notes
CL-nRCD-nRP					46-45-45			
Parameter				Symbol	min	max		
Read command to first data				tAA	16.000	22.222	ns	12
Activate to Read or Write command delay time				tRCD	16.000	-	ns	7
Row Precharge Time				tRP	16.000	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	48.000	-	ns	7,8
CAS Write Latency				CWL			nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRP-min (ns)[5]	Read CL[12]	Supported Frequency Table				
-	20.952	-	22	tCK(AVG)	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	ns	
3200AN	15.000	15.000	24	tCK(AVG)	RESERVED		ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	ns	
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED		ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED		ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	ns	
4400AN	14.545	14.545	32	tCK(AVG)	RESERVED		ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	ns	
4800AN	14.166	14.166	34	tCK(AVG)	RESERVED		ns	
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416		
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416		
5200AN	14.615	14.615	38	tCK(AVG)	RESERVED			
5600C	17.857	17.500	50	tCK(AVG)	0.357	<0.384		
5600BN	16.428	16.428	46	tCK(AVG)	0.357	<0.384		
5600B	16.428	16.071	46	tCK(AVG)	0.357	<0.384		
5600AN	14.285	14.285	40	tCK(AVG)	RESERVED			
Supported CL					22,26,28,30,32,36, 40,42,46,50		nCK	12

NOTE:

1) Minimum timing parameters are defined according to the rules in the Rounding Definitions and Algorithms section.
2) The translation of all timing parameters from ns values to nCK values shall follow the Rounding Algorithm. The translation of tAA to CL shall follow the explicit combinations listed in the Speed Bin Tables.
3) The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When selecting tCK(avg), requirements from the CL setting as well as requirements from the CWL setting shall be fulfilled.
4) 'Reserved' settings are not allowed. The user shall program a different value.
5. This column shows the intended native speed bin timings to be replaced and supported when down clocking. This column does not necessarily show the actual minimum speed bin timings allowed and supported when down clocking because the timings could be faster according to the Rounding Algorithm, depending on the specific speed bin and down clock frequency combination.
6) DDR5-3200 AC timings apply if the DRAM operates slower than the 2933 MT/s data rate. This is not limited to only the Speed Bin Table timings.
7) Parameters apply from tCK(avg)min to tCK(avg)max.
8) tRC(min) shall always be greater than or equal to tRAS(min) + tRP(min), and when using the appropriate rounding algorithms, nRC(min) shall always be greater than or equal to nRAS(min) + nRP(min).
9) tCK(avg).max of 1.010 ns (1980 MT/s data rate) is defined to allow for 1% SSC down-spreading at a data rate of 2000 MT/s according to JESD404-1.
10) Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC standard. The JEDEC standard does not require support for all speed bins within a given speed. The JEDEC standard requires meeting the parameters for a least one of the listed speed bins.
11) Any speed bin also supports functional operation at slower frequencies as shown in the table which are not subject to Production Tests but are verified by Design/Character -ization.
12) The CL Algorithm can be used to mathematically determine the valid CAS Latencies listed in the Speed Bin Tables. The CL Algorithm calculates supported CAS Latencies by rounding the operating frequency up to the next faster native speed bin (i.e., 3200 MT/s, 3600 MT/s...). Using the resulting tCK(AVG)min, and the bin target timings, the CL Algorithm then uses the Rounding Algorithm to calculate the valid CAS Latency. Because the DDR5 SDRAM specification only supports even CAS Latencies, odd CAS Latencies are rounded up to the next even CAS Latency. The 1980-2100 MT/s data rate always uses CL22. If tAA(corrected) or tRCDtRP(corrected) are violated, the CL Algorithm uses a slower combination of tAA(target) and tRCDtRP(target) to return slower valid CAS Latencies. The DDR5 SDRAM can support up to four valid CAS Latencies, CL(AN), CL(B), CL(BN), and CL(C), for a given frequency. tAA(corrected) and tRCDtRP(corrected) are calculated by reducing tAA(min), tRCD(min), and tRP(min) by the Rounding Algorithm correction factor. The proper setting of CL shall be determined by the memory controller, either by using the Speed Bin Tables, or by using the CL Algorithm, or by some other means. Refer to the Rounding Definitions and Algorithm section for more information.

11.0 IDD,IDDQ,IPPSPECIFICATION PARAMETERS AND TEST CONDITIONS

11.1 IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure 46 shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDDQ0, IPP0, IDD0F, IDDQ0F, IPP0F, IDD2N, IDDQ2N, IPP2N, IDD2NT, IDDQ2NT, IPP2NT, IDD2P, IDDQ2P, IPP2P, IDD3N, IDDQ3N, IPP3N, IDD3P, IDDQ3P, IPP3P, IDD4R, IDDQ4R, IPP4R, IDD4RC, IDD4W, IDDQ4W, IPP4W, IDD4WC, IDD5F, IDDQ5F, IPP5F, IDD5B, IDDQ5B, IPP5B, IDD5C, IDDQ5C, IPP5C, IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD7, IDDQ7, IPP7, and IDD8, IDDQ8, IPP8) are measured as time-averaged currents with all VDD balls of the DDR5 SDRAM under test tied together. Any IDDQ or IPP current is not included in IDD currents.
- IDDQ currents are measured as time-averaged currents with all VDDQ balls of the DDR5 SDRAM under test tied together. Any IDD or IPP current is not included in IDDQ currents.
- IPP currents are measured as time-averaged currents with all VPP balls of the DDR5 SDRAM under test tied together. Any IDD or IDDQ current is not included in IPP currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR5 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 47.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- “0” and “LOW” is defined as VIN <= VILAC(max).
- “1” and “HIGH” is defined as VIN >= VIHAC(min).
- “MID-LEVEL” is defined as inputs are VREF = 0.75 * VDDQ.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 51 through Table 60.
- IDD Measurements are done after properly initializing and training the DDR5 SDRAM. This includes but is not limited to setting

RON = RZQ/7 (34 Ohm in MR5);
RTT_NOM = RZQ/6 (40 Ohm in MR35);
RTT_WR = RZQ/2 (120 Ohm in MR34), only during IDD4 & IDD7 measurements, RTT_OFF for all other IDD measurements
RTT_PARK = Disable in MR33 and MR34;
Qoff = 0B (Output Buffer enabled) in MR5;
TDQS_t disabled in MR5;
CRC disabled in MR50;
DM disabled in MR5;
1N mode enabled and set CS assertion duration (MR2:OP[4]) as 1B in MR2, unless otherwise specified in the IDD, IDDQ and IPP patterns’ conditions definitions;

- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD, IDDQ or IPP measurement is started.
- TCASE defined as 0 - 95°C, unless stated in the specific condition definition table below.
- For all IDD, IDDQ and IPP measurement loop timing parameters, refer to the timing parameters defined in the spec to calculate the nCK required.

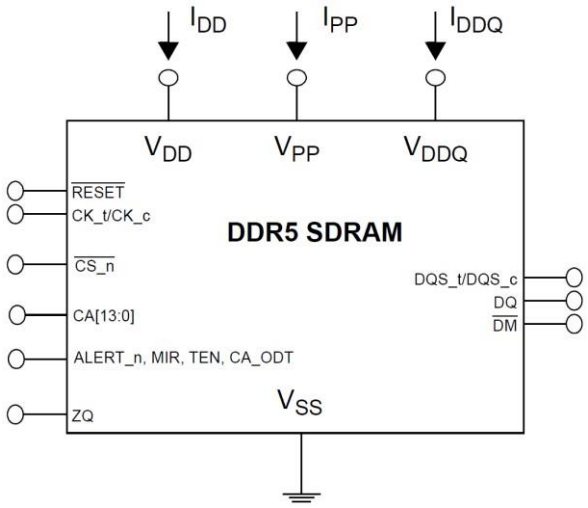


Figure 46. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

NOTE:
1) DIMM level Output test load condition may be different from above.

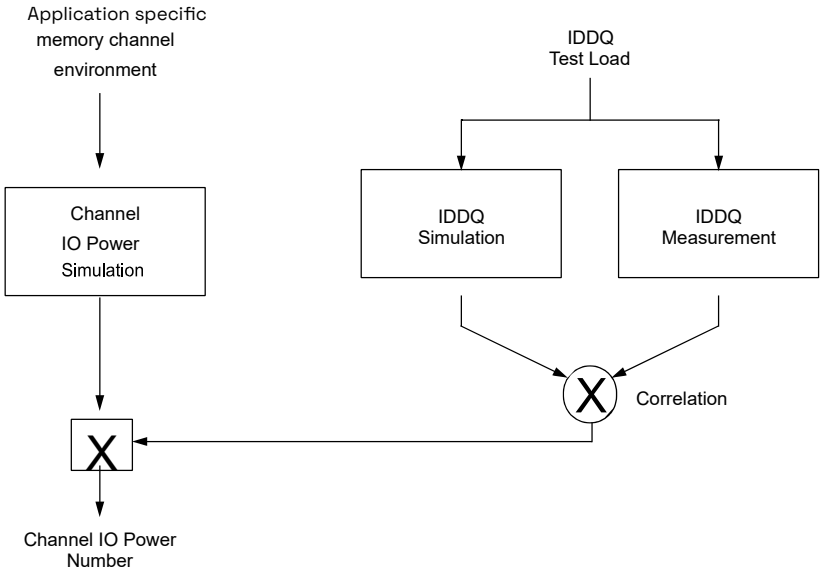


Figure 47. Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

[Table 53] Basic IDD, IDDQ and IPP Measurement Conditions

Symbol	Description
IDD0	Operating One Bank Active-Precharge Current External clock: On; tCK, nRC, nRAS, nRP, nRRD: refer to Chapter 13.3 Timing Parameters by Speed Grade; BL: 16[1]; CS_n: High between ACT and PRE; CA Inputs: partially toggling according to Table 54. Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 54); Output Buffer and RTT: Enabled in Mode Registers[2]; Pattern Details: see Table 54
IDD0Q	Operating One Bank Active-Precharge IDDQ Current Same condition with IDD0, however measuring IDDQ current instead of IDD current
IPP0	Operating One Bank Active-Precharge IPP Current Same condition with IDD0, however measuring IPP current instead of IDD current
IDD0F	Operating Four Bank Active-Precharge Current External clock: On; tCK, nRC, nRAS, nRP, nRRD: refer to Chapter 13.3 Timing Parameters by Speed Grade; BL: 16[1]; CS_n: High between ACT and PRE; CA Inputs: partially toggling according to Table 55; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with four bank active at a time: (see Table 55); Output Buffer and RTT: Enabled in Mode Registers[2]; Pattern Details: see Table 55
IDD0QF	Operating Four Bank Active-Precharge IDDQ Current Same condition with IDD0F, however measuring IDDQ current instead of IDD current
IPP0F	Operating Four Bank Active-Precharge IPP Current Same condition with IDD0F, however measuring IPP current instead of IDD current
IDD2N	Precharge Standby Current External clock: On; tCK: refer to Chapter 13.3 Timing Parameters by Speed Grade; CS_n: stable at 1; CA Inputs: partially toggling according to Table 56; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; Pattern Details: see Table 56
IDD2Q	Precharge Standby IDDQ Current Same condition with IDD2N, however measuring IDDQ current instead of IDD current
IPP2N	Precharge Standby IPP Current Same condition with IDD2N, however measuring IPP current instead of IDD current
IDD2NT	Precharge Standby Non-Target Command Current External clock: On; tCK: refer to Chapter 13.3 Timing Parameters by Speed Grade; BL: 16[1]; CS_n: High between WRITE commands; CS_n, CA Inputs: partially toggling according to Table 57; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; Pattern Details: see Table 57
IDD2NT (Optional)	Precharge Standby Non-Target Command IDDQ Current Same condition with IDD2NT, however measuring IDDQ current instead of IDD current

[Table 53] Basic IDD, IDDQ and IPP Measurement Conditions

Symbol	Description
IPP2NT (Optional)	Precharge Standby Non-Target Command IPP Current Same condition with IDD2NT, however measuring IPP current instead of IDD current
IDD2P	Precharge Power-Down Device in Precharge Power-Down, External clock: On; tCK: refer to Chapter 13.3 Timing Parameters by Speed Grade; CS_n: stable at 1 after Power Down Entry command; CA Inputs: stable at 1; CA11=H during the PDE command; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2];
IDDQ2P	Precharge Power-Down Same condition with IDD2P, however measuring IDDQ current instead of IDD current
IPP2P	Precharge Power-Down Same condition with IDD2P, however measuring IPP current instead of IDD current
IDD3N	Active Standby Current E xternal clock: On; tCK: refer to Chapter 13.3 Timing Parameters by Speed Grade; CS_n: stable at 1; CA Inputs: partially toggling according to Table 56; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2]; Pattern Details: see Table 56
IDDQ3N	Active Standby IDDQ Current Same condition with IDD3N, however measuring IDDQ current instead of IDD current
IPP3N	Active Standby IPP Current Same condition with IDD3N, however measuring IPP current instead of IDD current
IDD3P	Active Power-Down Current Device in Active Power-Down, External clock: On; tCK: refer to Chapter 13.3 Timing Parameters by Speed Grade; CS_n: stable at 1 after Power Down Entry command; CA Inputs: stable at 1; CA11=H during the PDE command; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2];
IDDQ3P	Active Power-Down IDDQ Current Same condition with IDD3P, however measuring IDDQ current instead of IDD current
IPP3P	Active Power-Down IPP Current Same condition with IDD3P, however measuring IPP current instead of IDD current
IDD4R	Operating Burst Read Current External clock: On; tCK, nCCD_S, CL: refer to Chapter 13.3 Timing Parameters by Speed Grade; BL: 16[1]; CS_n: High between RD; CA Inputs: partially toggling according to Table 56; Data IO: seamless read data burst with different data between one burst and the next one according to Table 58; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 58); Output Buffer and RTT: Enabled in Mode Registers[2]; Pattern Details: see Table 58
IDD4RC	Operating Burst Read Current with Read CRC Read CRC enabled[4]. Other conditions: see IDD4R
IDDQ4R	Operating Burst Read IDDQ Current Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IPP4R	Operating Burst Read IPP Current Same condition with IDD4R, however measuring IPP current instead of IDD current
IDD4W	Operating Burst Write Current External clock: On; tCK, nCCD_S_WR, CL: refer to Chapter 13.3 Timing Parameters by Speed Grade; BL: 16[1]; CS_n: High between WR; CA Inputs: partially toggling according to Table 59; Data IO: seamless write data burst with different data between one burst and the next one according to Table 59; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 59); Output Buffer and RTT: Enabled in Mode Registers[2]; Pattern Details: see Table 59
IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled[3], Other conditions: see IDD4W
IDDQ4W	Operating Burst Write IDDQ Current Same condition with IDD4W, however measuring IDDQ current instead of IDD current
IPP4W	Operating Burst Write IPP Current Same condition with IDD4W, however measuring IPP current instead of IDD current

Symbol	Description
IDD5B	Burst Refresh Current (Normal Refresh Mode) External clock: On; tCK, nRFC1: refer to Chapter 13.3 Timing Parameters by Speed Grade; BL: 16[1]; CS_n: High between REF; CA Inputs: partially toggling according to Table 60; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC1 (see Table 60); Output Buffer and RTT: Enabled in Mode Registers[2]; Pattern Details: see Table 60
IDDQ5B	Burst Refresh IDDQ Current (Normal Refresh Mode) Same condition with IDD5B, however measuring IDDQ current instead of IDD current
IPP5B	Burst Refresh IPP Current (Normal Refresh Mode) Same condition with IDD5B, however measuring IPP current instead of IDD current

[Table 53] Basic IDD, IDDQ and IPP Measurement Conditions

Symbol	Description
IDD5F	Burst Refresh Current (Fine Granularity Refresh Mode) tRFC=tRFC2, Other conditions: see IDD5B
IDDQ5F	Burst Refresh IDDQ Current (Fine Granularity Refresh Mode) Same condition with IDD5F, however measuring IDDQ current instead of IDD current
IPP5F	Burst Refresh IPP Current (Fine Granularity Refresh Mode) Same condition with IDD5F, however measuring IPP current instead of IDD current
IDD5C	Burst Refresh Current (Same Bank Refresh Mode) External clock: On; tCK, nRFCsb: refer to Chapter 13.3 Timing Parameters by Speed Grade; BL: 16[1]; CS_n: High between REF; CA Inputs: partially toggling according to Table 61; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFCsb (see Table 61); Output Buffer and RTT: Enabled in Mode Registers[2]; Pattern Details: see Table 61
IDDQ5C	Burst Refresh IDDQPP Current (Same Bank Refresh Mode) Same condition with IDD5C, however measuring IDDQ current instead of IDD current
IPP5C	Burst Refresh IPP Current (Same Bank Refresh Mode) Same condition with IDD5C, however measuring IPP current instead of IDD current
IDD6N	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; External clock: Off; CK_t and CK_c: HIGH; tCK, nCPDED: refer to Chapter 13.3 Timing Parameters by Speed Grade; BL: 16[1]; CS_n#: low; CA, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Disabled by the DRAM upon entry into Self- Refresh
IDDQ6N	Self Refresh IDDQ Current: Normal Temperature Range Same condition with IDD6N, however measuring IDDQ current instead of IDD current
IPP6N	Self Refresh IPP Current: Normal Temperature Range Same condition with IDD6N, however measuring IPP current instead of IDD current
IDD6E	Self Refresh Current: Extended Temperature Range) TCASE: 85 - 95°C; Extended4; External clock: Off; CK_t and CK_c: HIGH; tCK, nCPDED: refer to Chapter 13.3 Timing Parameters by Speed Grade; BL: 16[1]; CS_n: low; CA, Data IO: High; DM_n:stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Disabled by the DRAM upon entry into Self-Refresh
IDDQ6E	Self Refresh IDDQ Current: Extended Temperature Range Same condition with IDD6E, however measuring IDDQ current instead of IDD current
IPP6E	Self Refresh IPP Current: Extended Temperature Range Same condition with IDD6E, however measuring IPP current instead of IDD current

Symbol	Description
IDD7	Operating Bank Interleave Read Current External clock: On; tCK, nRC, nRAS, nRCD, nRRD_S, nFAW, tCCD_S CL: refer to Chapter 13.3 Timing Parameters by Speed Grade; BL: 16[1]; CS_n: High between ACT and RDA; CA Inputs: partially toggling according to Table 63; Data IO: read data bursts with different data between one burst and the next one according to Table 63; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, see Table 63; Output Buffer and RTT: Enabled in Mode Registers[2]; Pattern Details: see Table 63
IDDQ7	Operating Bank Interleave Read IDDQ Current Same condition with IDD7, however measuring IDDQ current instead of IDD current
IPP7	Operating Bank Interleave Read IPP Current Same condition with IDD7, however measuring IPP current instead of IDD current
IDD8	Maximum Power Saving Deep Power Down Current External clock: Off; CK_t and CK_c: HIGH; tCK, nCPDED: refer to Chapter 13.3 Timing Parameters by Speed Grade; BL: 16[1]; CS_n#: low; CA:High, DM_n: stable at 1; Bank Activity: All banks closed and device in MPSM deep power down mode5; Output Buffer and RTT: Enabled in Mode Registers[2]; Patterns Details: same as IDD6N but MPSM is enabled in mode register.
IDDQ8	Maximum Power Saving Deep Power Down IDDQ Current Same condition with IDD8, however measuring IDDQ current instead of IDD current
IPP8	Maximum Power Saving Deep Power Down IPP Current Same condition with IDD8, however measuring IPP current instead of IDD current
IDD9 (Optional)	MBIST Current Device in MBIST mode, External clock: On; CS_n: Stable at 1 after MBIST entry; CA Inputs: stable at 1; Data IO: VDDQ; Bank Activity: MBIST operation; Output Buffer and RTT: Enabled in Mode Registers[2];
IDDQ9 (Optional)	MBIST IDDQ Current Same condition with IDD9, however measuring IDDQ current instead of IDD current
IPP9 (Optional)	MBIST IPP Current Same condition with IDD9, however measuring IPP current instead of IDD current

NOTE:
1) Burst Length: BL16 fixed by MR0 OP[1:0]=00
2) Output Buffer Enable
- set MR5 OP[0] = 0] : Qoff = Output buffer enabled
- set MR5 OP[2:1] = 00]: Pull-Up Output Driver Impedance Control = RZQ/7
- set MR5 OP[7:6] = 00]: Pull-Down Output Driver Impedance Control = RZQ/7
RTT_Nom enable
- set MR35 OP[5:0] = 110110: RTT_NOM_WR = RTT_NOM_RD = RZQ/6
RTT_WR enable
- set MR34 OP[5:3] = 010 RTT_WR = RZQ/2
RTT_PARK disable
- set MR34 OP[2:0] = 000
3) WRITE CRC enabled
- set MR50 OP[2:1] = 11 4) Read CRC enabled
- set MR50:OP[0]=1
5) MPSM Deep Power Down Mode
- set MR2:OP[3]=1 if PDA Enumerate ID not equal to 15
- set MR2:OP[5]=1 if PDA Enumerate ID equal to 15

11.2 IDD0, IDDQ0, IPP0 Pattern

Executes Active and PreCharge commands with tightest timing possible while exercising all Bank and Bank Group addresses. Note 2 applies to the entire table.

[Table 54] IDD0, IDDQ0, IPP0

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L H	-	0x00000	0x0	0x00	0x0	
	1	DES	H	Toggling[1]					Repeat sequence to satisfy tRAS(min), truncate if required
	2	PREpb	L	-		0x0	0x00	0x0	
	3	DES	H	Toggling[1]					Repeat sequence to satisfy tPR(min), truncate if required
	4	ACT	L H	-	0x03FFF	0x0	0x00	0x0	
	5	DES	H	Toggling[1]					Repeat sequence to satisfy tRAS(min), truncate if required
	6	PREpb	L	-		0x0	0x00	0x0	
	7	DES	H	Toggling[1]					Repeat sequence to satisfy tPR(min), truncate if required
1	8-15	Repeat sub-loop 0, use BG[2:0]=0x1 instead							
2	16-23	Repeat sub-loop 0, use BG[2:0]=0x2 instead							
3	24-31	Repeat sub-loop 0, use BG[2:0]=0x3 instead							
4	32-39	Repeat sub-loop 0, use BG[2:0]=0x4 instead							skip for x16
5	40-47	Repeat sub-loop 0, use BG[2:0]=0x5 instead							skip for x16
6	48-55	Repeat sub-loop 0, use BG[2:0]=0x6 instead							skip for x16
7	56-63	Repeat sub-loop 0, use BG[2:0]=0x7 instead							skip for x16
8-15	64-127	Repeat sub loops 0-7, use BA[1:0]=0x1 instead							
16-23	128-191	Repeat sub loops 0-7, use BA[1:0]=0x2 instead							
24-31	192-255	Repeat sub loops 0-7, use BA[1:0]=0x3 instead							
...	...	Repeat sub loops 0-31 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

NOTE :
1) Utilize DESELECTs between commands while toggling all C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern

11.3 IDDOF, IDDQOF, IPPOF Pattern

Executes a rolling four bank group Active and PreCharge commands per tRC time while exercising all Bank, Bank, Group and CID addresses. Note 2 applies to the entire table.

[Table 55] IDDOF, IDDQOF, IPPOF

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L H		0x00000	0x0	0x00	0x0	
	1	DES	H	Toggling[1]					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	2	ACT	L H		0x00000	0x0	0x01	0x0	
	3	DES	H	Toggling[1]					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	4	ACT	L H		0x00000	0x0	0x02	0x0	
	5	DES	H	Toggling[1]					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	6	ACT	L H		0x00000	0x0	0x03	0x0	
	7	DES	H	Toggling[1]					Repeat to satisfy tRAS(min) from Sequence 0
	8	PREpb	L			0x0	0x00	0x0	
	9	DES	H	Toggling[1]					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	10	PREpb	L			0x0	0x01	0x0	
	11	DES	H	Toggling[1]					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	12	PREpb	L			0x0	0x02	0x0	
	13	DES	H	Toggling[1]					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	14	PREpb	L			0x0	0x03	0x0	
	15	DES	H	Toggling[1]					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	16	DES	H	Toggling[1]					Repeat for tRC(min) from Sequence 0 first ACTIVATE. This will be zero DESELECTS for speed 4000Mbps and slower.
1	17-33	Repeat sub-loop 0, use Row Address = 0x03FFF for the ACT instead							
2-3	34-67	Repeat sub-loop 0-1, use BG[2:0]=0x4,0x5,0x6,0x7 instead of 0x0,0x1,0x2,0x3							skip for x16
4-7	68-101	Repeat sub-loops 0-3, use BA[1:0]=0x1 instead							
8-11	102-135	Repeat sub-loops 0-3, use BA[1:0]=0x2 instead							
12-15	136-169	Repeat sub-loops 0-3, use BA[1:0]=0x3 instead							
...	...	Repeat sub loops 0-15 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

NOTE:

1) Utilize DESELECTs between commands while toggling C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.

11.4 IDD2N, IDD3N Pattern

Executes DESELECT commands while exercising all command/address pins in a predefined pattern. All notes apply to entire table. **[Table 56] IDD2N, IDDQ2N, IPP2N, IDD3N, IDDQ3N, IPP3N**

Sequence	Command	CS	C/A [13:0]
0	DES	H	0x0000
1	DES	H	0x3FFF
2	DES	H	0x3FFF
3	DES	H	0x3FFF

NOTE:
1) Data is pulled to VDDQ
2) DQS_t and DQS_c are pulled to VDDQ
3) Command / Address ODT is disabled
4) Repeat sequence 0 through 3
5) All banks of all logical ranks mimic the same test condition

11.5 IDD2NT, IDDQ2NT, IPP2NT Pattern

Executes Non-Target WRITE commands simulating Rank to Rank timing while exercising all C/A bits. Notes 3-6 apply to entire table.

[Table 57] IDD2NT, IDDQ2NT, IPP2NT

Sequence	Command	CS_n	C/A [13:0]	Special Instructions
0	WRITE	L	0x002D	All valid C/A inputs to VSS
		L	0x0000	
1	DES	H	Toggling[2]	Repeat sequence to meet 1*tCCD_S(min), truncate if required
2	WRITE	L	0x3FED	All valid C/A inputs to VDDQ
		L	0x3FFF	
3	DES	H	Toggling[2]	Repeat sequence to meet 1*tCCD(min), truncate if required

NOTE:
1) WRITE with CS_n=L on both cycles indicated a non-target WRITE
2) Utilize DESELECTs between commands while toggling C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern
3) Time between Non-Target WRITEs reflect tCCD_S (min) for one rank
4) DQ signals are VDDQ
5) DQS_t, DQS_c are VDDQ
6) Repeat 0 through 3

11.6 IDD4R, IDDQ4R, IPP4R Pattern

Executes READ commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses. Notes 2-9 apply to entire table **[Table 58] IDD4R, IDDQ4R, IPP4R**

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
0	0	READ	L H	-	0x000	0x00	0x0	0x0	Pattern A	All "Valid" inputs = VDDQ
	1	DES	H	Toggling[1]	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
1	2	READ	L H	-	0x3F0	0x00	0x1	0x0	Pattern B	All "Valid" inputs = VDDQ
	3	DES	H	Toggling[1]	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead								skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								skip for x16
8	16	READ	L H	-	0x3F0	0x00	0x0	0x0	Pattern B	All "Valid" inputs = VDDQ
	17	DES	H	Toggling[1]						Repeat sequence to satisfy tCCD_S(min), truncate if required
9	18	READ	L H	-	0x000	0x00	0x1	0x0	Pattern A	All "Valid" inputs = VDDQ
	19	DES	H	Toggling[1]						Repeat sequence to satisfy tCCD_S(min), truncate if required
10	20-21	Repeat sub-loop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat sub-loop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat sub-loop 8, use BG[2:0]=0x4 instead								skip for x16
13	26-27	Repeat sub-loop 9, use BG[2:0]=0x5 instead								skip for x16
14	28-29	Repeat sub-loop 8, use BG[2:0]=0x6 instead								skip for x16
15	30-31	Repeat sub-loop 9, use BG[2:0]=0x7 instead								skip for x16
16-31	32-33	Repeat sub-loops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat sub-loops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat sub-loops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat sub-loops 0-63 for each 3DS logical rank, if applicable								CID[2:0]=0x1-0x7

NOTE:

1) Utilize DESELECTs between commands while toggling all C/A bits 100% each cycle (0x3FFF, 0x0000, 0x3FFF, 0x0000...) per the 4-cycle sequence defined in the IDD2N,
IDD3N pattern

2) READs performed with Auto Precharge = H, Burst Chop = H

3) Row address is set to 0x0000
4) Data reflects burst length of 16
5) Data Pattern A for x4: 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0x0, 0xF
6) Data Pattern B for x4: 0xF, 0x0, 0x0, 0xF, 0xF, 0x0, 0xF, 0x0, 0x0, 0xF, 0xF, 0x0, 0xF, 0x0, 0xF, 0x0
7) Data Pattern for x8 each beat will reflect two like nibbles (Data Pattern A = 0x00, 0xFF, 0xFF...)
8) Data Pattern for x16 each beat will reflect two like bytes (Data Pattern A = 0x0000, 0xFFFF, 0xFFFF...)
9) Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state

11.7 IDD4W, IDDQ4W, IPP4W Pattern

Executes WRITE commands with tightest timing possible while exercising all Bank, Bank Group and CDI CID addresses. Notes 2-6 apply to entire table.

[Table 59] IDD4W, IDDQ4W, IPP4W

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
0	0	WRITE	L H	-	0x000	0x00	0x0	0x0	Pattern A	All “Valid” inputs = VDDQ
	1	DES	H	Toggling[1]	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
1	2	WRITE	L H	-	0x3F0	0x00	0x1	0x0	Pattern B	All “Valid” inputs = VDDQ
	3	DES	H	Toggling[1]	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 i nstead								skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								skip for x16
8	16	WRITE	L H	-	0x3F0	0x00	0x0	0x0	Pattern B	All “Valid” inputs = VDDQ
	17	DES	H	Toggling[1]	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
9	18	WRITE	L H	-	0x000	0x00	0x1	0x0	Pattern A	All “Valid” inputs = VDDQ
	19	DES	H	Toggling[1]	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
10	20-21	Repeat sub-loop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat sub-loop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat sub-loop 8, use BG[2:0]=0x4 instead								skip for x16
13	26-27	Repeat sub-loop 9, use BG[2:0]=0x5 instead								skip for x16
14	28-29	Repeat sub-loop 8, use BG[2:0]=0x6 instead								skip for x16
15	30-31	Repeat sub-loop 9, use BG[2:0]=0x7 instead								skip for x16
16-31	32-33	Repeat sub-loops 0-15, use BA[1:0]=0x1 instead								

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
32-47	34-35	Repeat sub-loops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat sub-loops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat sub-loops 0-63 for each 3DS logical rank, if applicable								CID[2:0]=0x1-0x7

NOTE:
1) Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern
2) WRITEs performed with Auto Precharge = H, Burst Chop = TBD
3) Row address is set to 0x0000
4) Data reflects burst length of 16
5) Refer to IDD4R measurement loop table for data pattern definition
6) Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state

11.8 IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F Pattern

Executes Refresh (all Banks) command at minimum tRFC. Notes 3-6 apply to entire table.

[Table 60] IDD5B, IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F

Sub-Loop	Command	CS	C/A [13:0]	CA8	CID[2:0]	Special Instructions
0	REFab	L	-	H	0x0	All “valid” inputs = VDDQ
1	DES	H	Toggling[1]	-	-	Repeat sequence to satisfy tRFC(min), truncate if required
2	REFab	L	-	H	0x0	All “valid” inputs = VDDQ
3	DES	H	Toggling[1]	-	-	Repeat sequence to satisfy tRFC(min), truncate if required
...	Repeat sequence 0-3 for each 3DS logical rank, if applicable					CID[2:0]=0x1-0x7

NOTE:
1) Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern
2) For IDD5B, use tRFC1(min). For IDD5F, use tRFC2(min)
3) DQ signals are VDDQ
4) All banks of all “non-target” logical ranks are Idd2N condition
5) Where C/A[13:0] column is not populated, refer to command truth table, CA8, and CID columns for the C/A state 6) Must set CA8=H on REFab commands to indicate 1X refresh rate on devices that support RIR

11.9 IDD5C, IDDQ5C and IPP5C Patterns

Executes Refresh (Same Bank) command at minimum tRFCsb. Notes 2-5 apply to entire table.

[Table 61] IDD5C, IDDQ5C, IPP5C

Sub-Loop	Command	CS	C/A [13:0]	CA8	BA[1:0]	CID[2:0]	Special Instructions
0	REFsb	L	-	H	0x0	0x0	
1	DES	H	Toggling[1]	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
2	REFsb	L	-	H	0x1	0x0	
3	DES	H	Toggling[1]	-		-	Repeat sequence to satisfy tRFCsb(min), truncate if required
4	REFsb	L	-	H	0x2	0x0	

Sub-Loop	Command	CS	C/A [13:0]	CA8	BA[1:0]	CID[2:0]	Special Instructions
5	DES	H	Toggling[1]	-		-	Repeat sequence to satisfy tRFCsb(min), truncate if required
6	REFsb	L	-	H	0x3	0x0	
7	DES	H	Toggling[1]	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
...	Repeat sequence 0-7 for each 3DS logical rank, if applicable						CID[2:0]=0x1-0x7

NOTE:
1) Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern 2) DQ signals are VDDQ
3) All banks of all “non-target” logical ranks are Idd2N condition
4) Where C/A[13:0] column is not populated, refer to command truth table, CA8, and CID columns for the C/A state
5) All banks of all “non-target” logical ranks are Idd2N condition

11.10 IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R Pattern

All notes apply to entire table.

[Table 62] IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R

Sub-Loop	Command	Clock	CS	C/A[13:0]	Special Instructions
0	SRE	Valid	L	0x3BF7	Clocks must be valid tCKLCS(min) time
1	DES	Valid	H	0x3FFF	Repeat sequence to satisfy tCPDED(min), truncate if required
2	All C/A=H	Valid	L	0x3FFF	
3	All C/A=H	CK_t = CK_c = H	L	0x3FFF	Repeat sequence indefinitely

NOTE:
1) Data is pulled to VDDQ
2) DQS_t and DQS_c are pulled to VDDQ
3) ODT disabled in Mode Registers

11.11 IDD7, IDDQ7 and IPP7 Patterns

Executes ACTVATE, READ/A commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses. Notes 2-6 apply to entire table.

[Table 63] IDD7, IDD7Q, IPP7

Sub-Loop	Sequence	Command	CS	C/A [13:0]	Row Address [17:0]	Column Addres s [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
0	0	ACT	L H	-	0x00000	-	0x0	0x0	0x0	-	
	1	DES	H	Toggling[1]							Repeat sequence to satisfy tRRD_S(min), tFAW(min), and tRCD(min). Truncate if required.
1	2	ACT	L H	-	0x03FFF	-	0x0	0x1	0x0	-	
	3	DES	H	Toggling[1]							Repeat sequence to satisfy tRRD_S(min), tFAW(min), and tRCD(min). Truncate if required.
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead									
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead									
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead									skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead									skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead									skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead									skip for x16
8	16	RDA	L H	-	-	0x3F0	0x0	0x0	0x0	Pattern A	
	17	ACT	L H	-	0x00000	-	0x1	0x0	0x0	-	
	18	DES	H	Toggling[1]							Repeat sequence to satisfy tCCD_S(min), tFAW(min), and tRCD(min). Truncate if required.
9	19	RDA	L H	-	-	0x000	0x0	0x1	0x0	Pattern B	
	20	ACT	L H	-	0x03FFF	-	0x1	0x1	0x0	-	
	21	DES	H	Toggling[1]							Repeat sequence to satisfy tCCD_S(min), tFAW(min), and tRCD(min). Truncate if required.
10	22-24	Repeat sub-loop 8, use BG[2:0]=0x2 instead									
11	25-27	Repeat sub-loop 9, use BG[2:0]=0x3 instead									
12	28-30	Repeat sub-loop 8, use BG[2:0]=0x4 instead									skip for x16
13	31-33	Repeat sub-loop 9, use BG[2:0]=0x5 instead									skip for x16
14	34-36	Repeat sub-loop 8, use BG[2:0]=0x6 instead									skip for x16

Sub-Loop	Sequence	Command	CS	C/A [13:0]	Row Address [17:0]	Column Addres s [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
15	37-39	Repeat sub-loop 9, use BG[2:0]=0x7 instead									skip for x16
16-23	40-64	epeat sub-loops 8-15, use BA[1:0]=0x1 for the RDA and BA[1:0]=0x2 for the CT									
24-31	65-89	epeat sub-loops 8-15, use BA[1:0]=0x2 for the RDA and BA[1:0]=0x3 for the CT									
32-39	90-114	epeat sub-loops 8-15, use BA[1:0]=0x3 for the RDA and BA[1:0]=0x0 for the CT									
...	...	Repeat sub-loops 0-18 for each 3DS logical rank, if applicable									CID[2:0]=0x1-0x7

NOTE:
1) Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern
2) READs performed with Auto Precharge = H, Burst Chop = H
3) x8 or x16 may have different Bank or Bank Group Address
4) Data reflects burst length of 16
5) Refer to IDD4R measurement loop table for data pattern definition

12.0 IDD SPEC TABLE

IDD values are for typical operating range of voltage and temperature unless otherwise noted.

Symbol	ZMS5WMC3C1J0B46SPG: 1Rx16 8GB Module	ZMS5WMC8C2J0B46SPG: 1Rx8 16GB Module	ZMS5WMC8C4J0B46SPG: 2Rx8 32GB Module	Unit
	DDR5-5600	DDR5-5600	DDR5-5600	
	46-45-45	46-45-45	46-45-45	
	IDD Max.	IDD Max.	IDD Max.	
	VDD 1.1V, VDDQ 1.1V, VPP 1.8V	VDD 1.1V, VDDQ 1.1V, VPP 1.8V	VDD 1.1V, VDDQ 1.1V, VPP 1.8V	
IDD0	TBD	TBD	TBD	mA
IDD0F	TBD	TBD	TBD	mA
IDD2N	TBD	TBD	TBD	mA
IDD2NT	TBD	TBD	TBD	mA
IDD2P	TBD	TBD	TBD	mA
IDD3N	TBD	TBD	TBD	mA
IDD3P	TBD	TBD	TBD	mA
IDD4R	TBD	TBD	TBD	mA
IDD4W	TBD	TBD	TBD	mA
IDD5B	TBD	TBD	TBD	mA
IDD5F	TBD	TBD	TBD	mA
IDD5C	TBD	TBD	TBD	mA
IDD6N	TBD	TBD	TBD	mA
IDD7	TBD	TBD	TBD	mA
IDD8	TBD	TBD	TBD	mA

NOTE :

1) DIMM IDD SPEC is based on the condition that de-actived rank (IDLE) is IDD2N. Please refer to Table.
2) IDD current measure method and detail patterns are described on DDR5 component datasheet.
3) Module IDD is based on PMIC 5V input current, each IDD parameter includes all IDD/IDDQ/IPP of DRAM and PMIC efficiency.

[Table 64] DIMM Operating Status

IDD Status	Operating Rank	De-actived rank
IDD0	IDD0	IDD2N
IDD0F	IDD0F	IDD2N
IDD2N	IDD2N	IDD2N
IDD2NT	IDD2NT	IDD2N
IDD2P	IDD2P	IDD2P
IDD3N	IDD3N	IDD2N
IDD3P	IDD3P	IDD2P
IDD4R	IDD4R	IDD2N
IDD4W	IDD4W	IDD2N
IDD5B	IDD5B	IDD2N
IDD5F	IDD5F	IDD2N
IDD5C	IDD5C	IDD2N
IDD6N	IDD6N	IDD6N
IDD7	IDD7	IDD2N
IDD8	IDD8	IDD8

13.0 INPUT/OUTPUT CAPACITANCE

[Table 65] Silicon Pad I/O Capacitance

Symbol	Parameter	DDR5-4400 to 4800		DDR5-5200 to 5600		Unit	NOTE
		min	max	min	max		
CIO	Input/output capacitance (DQ, DM_n, DQS_t, DQS_c, TDQS_t, TDQS_c)	0.35	0.9	0.35	0.85	pF	1,2
CDIO	Input/output capacitance delta (DQ, DM_c)	-0.1	0.1	-0.1	0.1	pF	1,2,8
CDDQS	Input/output capacitance delta (DQS_t and DQS_c)		0.04		0.04	pF	1,2,4
CCK	Input capacitance (CK_t and CK_c)	0.2	0.6	0.2	0.55	pF	1,2
CDCK	Input capacitance delta (CK_t and CK_c)		0.05		0.05	pF	1,2,3
CI	Input capacitance (CS_n & CA[13:0] pins only)	0.2	0.6	0.2	(CI Option1) 0.55 (CI Option2) 0.5	pF	1,2,5,1 2
CDI_ CS_n	Input capacitance delta (CS_n pin only)	-0.1	0.1	-0.1	0.1	pF	1,2,6
CDI_ CA	Input capacitance delta (CA[13:0] pins only)	-0.1	0.1	-0.1	0.1	pF	1,2,7
CALERT	Input/output capacitance of ALERT	0.3	1.5	0.3	1.5	pF	1,2
CLoopback	Input/output capacitance of Loopback (LBDQ, LBDQS)	0.3	1.0	0.3	1.0	pF	1,2
CTEN	Input capacitance of TEN	0.2	2.3	0.2	2.3	pF	1,2,9
CZQ	Input capacitance of ZQ	-	5	-	5	pF	1,2,11
CSTRAP	Input capacitance of MIR, CAI, CA_ODT pins	-	10	-	10	pF	1,2,10

NOTE :

1) This parameter is not subject to production test. This parameter is measured by using vendor specific measurement methodology.
2) This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
3) Absolute value CIO(CK_t)-CIO(CK_c).
4) Absolute value of CIO(DQS_t)-CIO(DQS_c).
5) CI applies to CS_n and CA[13:0].
6) CDI_CS_n = CI(CS_n)-0.5*(CI(CK_t)+CI(CK_c)). 7) CDI_CA = CI(CA[13:0])-0.5*(CI(CK_t)+CI(CK_c)).
8) CDIO = CIO(DQ,DM)-Avg(CIO(DQ,DM)).
9) TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.
10) MIR, CAI, and CA_ODT are strap pins used to configure module or point to point use cases depending on power, signal integrity, and termination requirements. No active AC signaling requirements defined for these pins.
11) Maximum external load capacitance on ZQ pin: 25pF. The ZQ functionality / accuracy with the max capacitive load is characterized.
12) CI Options are incorporated VcIVW in table 9 in Section 8.2.

14.0 tREFI and tRFC Parameters

The maximum average refresh interval (tREFI) requirement for the DDR5 SDRAM depends on the refresh mode setting (Normal or FGR), and the device's case temperature (Tcase). When the refresh mode is set to Normal Refresh mode, REFab commands are issued (tRFC1), and Tcase<=85°C, the maximum average refresh interval (tREFI1) is tREFI. When the refresh mode is set to FGR mode, REFab commands are issued (tRFC2) and Tcase<=85°C, the maximum average refresh interval (tREFI2) is tREFI/2. This same tREFI/2 interval value is also appropriate if the refresh mode is set to Normal Refresh mode and REFab commands are issued (tRFC1) but 85°C<Tcase<=95°C. Finally, if the refresh mode is set to FGR mode, REFab commands are issued (tRFC2), and 85°C<Tcase<=95°C, the maximum average refresh interval (tREFI2) is tREFI/4.

The DDR5 SDRAM includes an optional method for the host to indicate when Refresh commands are being issued at the 2x (tREFI2) refresh interval rate. The 2x Refresh Interval Rate indicator (MR4:OP[3]) alerts the DRAM if the host supports the refresh interval rate indication as part of the REF command using CA8. If enabled (MR4:OP[3]=1), the host will issue 1x REF commands with CA8=H (Tcase<=85°C), and the host will issue 2x REF commands with CA8=L (Tcase any allowable temperature). MR4:OP[3] is a Status Read/Write "SR/W" MR bit which shows DDR5 SDRAM support of this optional feature.
Reading MR4:OP[3] will return a "1" if the 2x Refresh Interval Rate indicator is supported. A "0" will be returned if not supported.
tREFI is based on the 8,192 refresh commands that need to be issued within the baseline tREF=32ms refresh period on the DDR5 SDRAM.

[Table 66] tREFI parameters for REFab and REFsb Commands

Command	Refresh Mode	S ımbol & Range		Expression	Value	Unit	Notes
REFab	Normal	tREFI1	0°C <= TCASE <= 85°C	tREFI	3.9	us	
			85°C < TCASE <= 95°C	tREFI/2	1.95	us	
REFab	Fine Granularity	tREFI2	0°C <= TCASE <= 85°C	tREFI/2	1.95	us	
			85°C < TCASE <= 95°C	tREFI/4	0.975	us	
REFsb	Fine Granularity	tREFIsb	0°C <= TCASE <= 85°C	tREFI/(2*n)	1.95/n	us	1
			85°C < TCASE <= 95°C	tREFI/(4*n)	0.975/n	us	1

NOTE :
1) *n* is the number of banks in a bank group (e.g. 8G: n=2; 16G: n=4).

[Table 67] tRFC parameters by device density

Refresh Mode	Symbol	16Gb	Unit	Notes
Normal Refresh (REFab)	tRFC1(min)	295	ns	
Fine Granularity Refresh (REFab)	tRFC2(min)	160	ns	
Same Bank Refresh (REFsb)	tRFCsb(min)	130	ns	

[Table 68] Same Bank Refresh parameters

Refresh Mode	Symbol	16Gb	Unit	Notes
Same Bank Refresh to ACT delay	tREFSBRD_slr(min)	30	ns	

15.0 TIMING PARAMETERS BY SPEED GRADE

15.1 Timing Parameters by Speed Bin

Speed		DDR5-4400		DDR5-4800		DDR5-5200		DDR5-5600		Units	Notes
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
Clock Timing											
Average Clock Period	tCK(avg)	0.454	-	0.416	-	0.384		0.357	-	ns	1
Command and Address Timing											
Read to Read command delay for same bank group	tCCD_L	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)		max(8nCK, 5ns)	-	nCK,ns	
Write to Write command delay for same bank group	tCCD_L_WR	max(32nCK, 20ns)	-	max(32nCK, 20ns)	-	max(32nCK, 20ns)		max(32nCK, 20ns)	-	nCK,ns	
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	Max(16nCK, 10ns)	-	Max(16nCK, 10ns)	-	Max(16nCK, 10ns)		Max(16nCK, 10ns)	-	nCK,ns	
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE								nCK,ns	3,5,6
Write to Read command delay for same bank group	tCCD_L_ WTR	CWL + WBL/2 + Max(16nCK,10ns)								nCK,ns	4,6
Read to Read command delay for different bank group	tCCD_S	8	-	8	-	8		8	-	nCK	
Write to Write command delay for different bank group	tCCD_S_WR	8	-	8	-	8		8	-	nCK	
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE								nCK,ns	3,5,6
Write to Read command delay for different bank group	tCCD_S_ WTR	CWL + WBL/2 + Max(4nCK,2.5ns)								nCK,ns	4,6
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP								nCK,ns	2,4,6
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)		max(8nCK, 5ns)	-	nCK,ns	
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)		max(8nCK, 5ns)	-	nCK,ns	
Activate to Activate command delay to differ- ent bank group for 1KB page size	tRRD_S(1K)	8	-	8	-	8		8	-	nCK	
Activate to Activate command delay to differ- ent bank group for 2KB page size	tRRD_S(2K)	8	-	8	-	8		8	-	nCK	
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 16.000ns)	-	Max(32nCK, 14.545ns)	-	Max(32nCK, 14.545ns)		Max(32nCK, 12.307ns)	-	nCK, ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 20.000ns)	-	Max(40nCK, 18.181ns)	-	Max(40nCK, 18.181ns)		Max(40nCK, 15.384ns)	-	nCK, ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)		Max(12nCK, 7.5ns)	-	nCK,ns	
Precharge to Precharge command delay	tPPD	2	-	2	-	2		2	-	nCK	7
Write recovery time	tWR	30	-	30	-	30		30	-	ns	

NOTE:

1) tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.
2) tCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + tWR(min) - tRTP(min), and when using the appropri- ate rounding algorithms, nCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + nWR(min) - nRTP(min).
3) RBL: Read burst length associated with Read command.
RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode.
4) WBL: Write burst length associated with Write command

WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode.
WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode.
5) The following is considered for tRTW equation.
1tCK needs to be added due to tDQS2CK.
Read DQS offset timing can pull in the tRTW timing 1tCK needs to be added when 1.5tCK
postamble. 6) CWL=CL-2
7) This parameter only specifies minimum values (there is no maximum value). The maximum value cells have been merged in the table to improve legibility.

15.2 DDR5 Function Matrix

DDR5 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

[Table 69] Function Matrix (By ORG. V:Supported, Blank:Not supported)

Functions	x8	x16	NOTE
Write Leveling	V	V	
Temperature controlled Refresh	V	V	
Fine Granularity Refresh	V	V	
Same Bank Refresh	V	V	
Refresh for Management			
Data Mask	V	V	
Command Address Inversion	V	V	
TDQS	V	V	
ZQ calibration	V	V	
DQ Vref Training	V	V	
Per DRAM Addressability	V	V	
Mode Register Readout	V	V	
WRITE CRC	V	V	
READ CRC	V	V	
Programmable Preamble/Postamble	V	V	
Maximum Power Saving Mode	V	V	
Connectivity Test Mode	V	V	
Bit Error Rate Test	V	V	
Package Output Driver Test Mode	V	V	
3DS			
CA Training Mode	V	V	
CS Training Mode	V	V	
DQS interval Oscillator	V	V	
ECC Transparency and Error Scrub	V	V	
Lookback	V	V	
Duty Cycle Adjuster	V	V	

16.0 DDR5 MODULE RANK AND CHANNEL TIMINGS

16.1 Module Rank and Channel Limitations for DDR5 DIMMs

To achieve efficient module power supply design for JEDEC-standard DDR5 DIMMs, minimum timings as well as limitations in the number of DRAMs are provided for Refresh, and Write operations occurring on a single module. As well, since these modules are organized as two independent 36-bit or 40-bit channels (32 bits for non-ECC DIMMs), additional restrictions apply in order to limit localized power delivery noise on the module. To provide best performance, the different channels may initiate commands on the same cycle provided the rank to rank timings are met, the maximum number of DRAMs in a given activity is not exceeded, and the applicable component timings shown elsewhere in this specification are met. The timing and operational relationships for DDR5 DIMMs are shown in Table 68 below.

[Table 70] DDR5 Module Rank and Channel Timings for DDR5 DIMMs

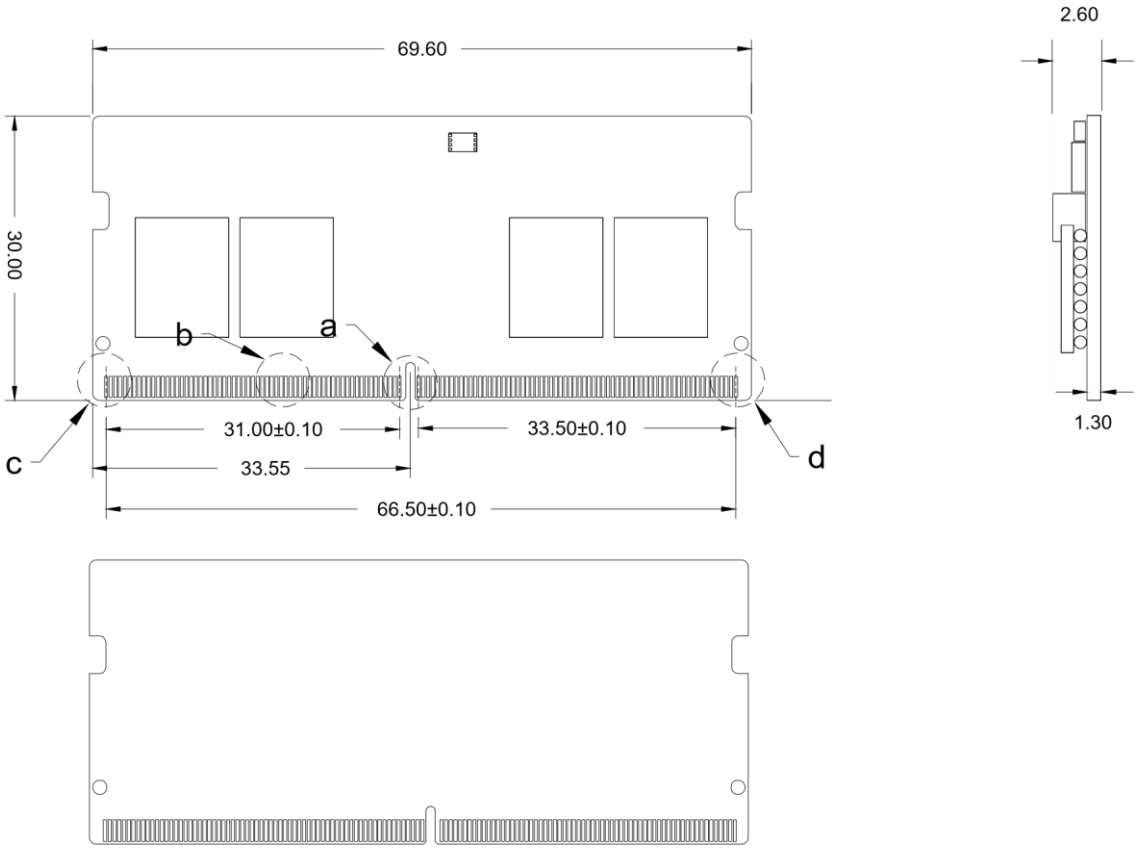
DIMM Configuration	Maximum number of DRAM die in simultaneous or overlapping activity			
	Refresh (All-Bank Refresh)		Write, Write-Pattern	
	Die per Physical Rank	Die per DIMM	Die per Channel	Die per DIMM
SR x16	No restriction			
DR x16	No restriction		2	4
SR x8	No restriction			
DR x8	No restriction		5	10
SR x4	No restriction			
DR x4	No restriction		10	20
Notes	1, 2, 3, 4, 7, 8, 9		1, 5, 6, 7, 9	

NOTE:
1) Any combination of commands with up to the maximum of die per channel and per DIMM, per condition is allowed 2) Refresh commands to different channels do not require stagger
3) tRFC_dlr must be met for refresh commands to different logical ranks within a package rank on the same channel
4) Any DRAM is considered to be in Refresh mode until tRFC time has been met
5) tCCD parameters must be met for Write and Write-Pattern commands to different logical ranks or physical ranks within the same channel; no overlapping write data bus activity is allowed on two physical or logical ranks within the same channel
6) Write and Write-Pattern commands to different channels do not require stagger
7) Each rank consists of one group of DRAMs making up a 36 or 40 bit channel (32 bits for non-ECC DIMMs)
8) These restrictions only apply to explicit all-banks refresh commands (REFab) and not to self-refresh entry or exit
9) Restrictions apply to DIMMs built with JEDEC PMICXXXX, but may not apply to DIMMs built with higher current capacity PMICs

17.0 PHYSICAL DIMENSIONS

17.1 1Gx16 based x64 Module (1 Rank) - ZMS5WMC3C1J0B46SPG

Units : mm



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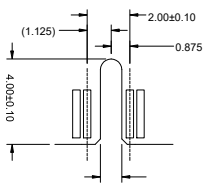

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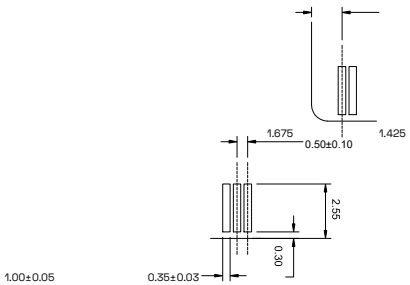
DETAIL c



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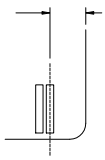
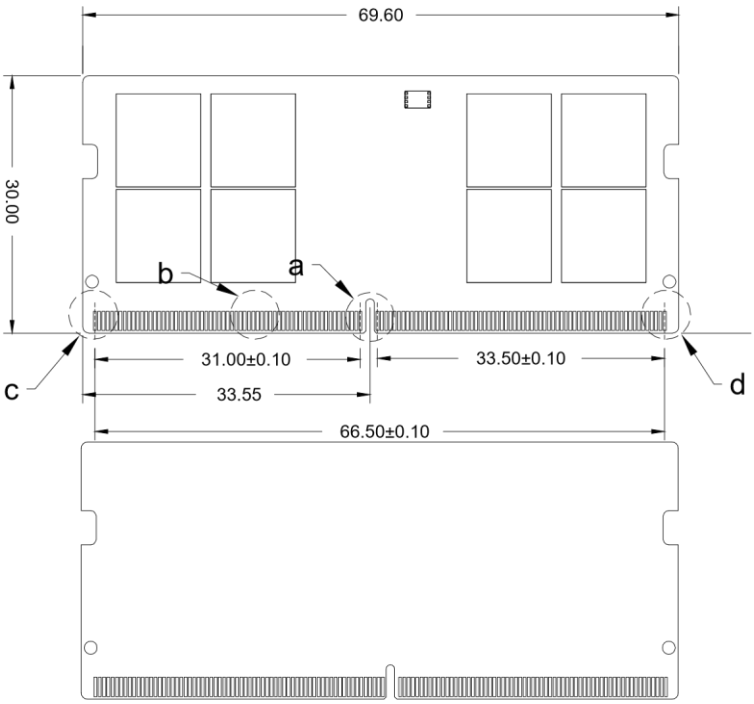
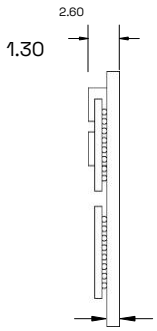


NOTE: Tolerances on all dimensions ±0.15 unless otherwise specified

17.2 2Gx8 based x64 Module (1 Rank) - ZMS5WMC8C2J0B46SPG

Units : mm





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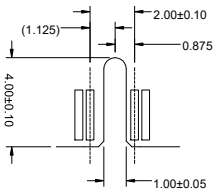

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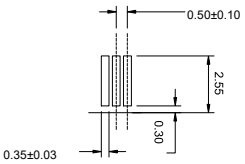

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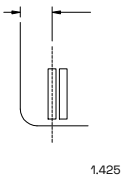

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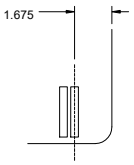
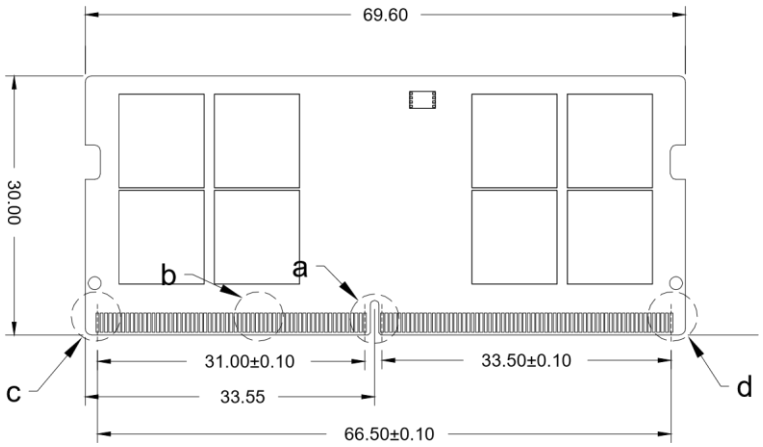
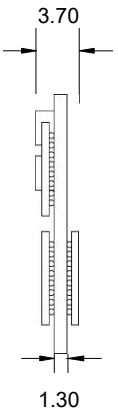


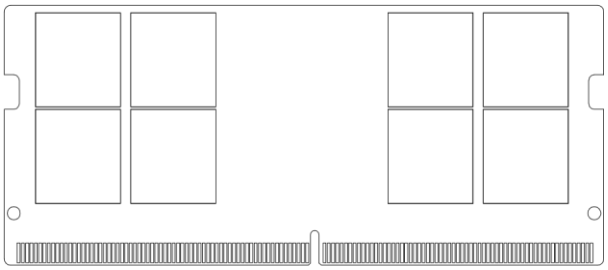
NOTE: Tolerances on all dimensions ±0.15 unless otherwise specified

17.3 2Gx8 based x64 Module (2 Ranks) - ZMS5WMC8C4J0B46SPG

Units : mm







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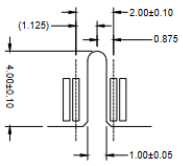

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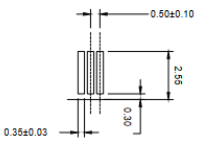

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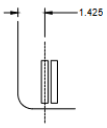

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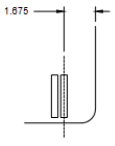

NOTE: Tolerances on all dimensions ±0.15 unless otherwise specified

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