zilia technologies

FSB0C256G-B7C0700K
FSB0C512G-B7C0700K
April 04th, 2025

M.2 22x80 NVMe PCIe SSD specification

April 04th, 2025

Rev 1.0

Key Features

Capacity

- 256GB/512GB

Form Factor

- M.2 2280

Features

- PCIe Gen 4 16Gb/s interface with up to 4 lanes
- Compliant with NVMe Revision 1.4
- Supporting host memory buffer
- Supporting initial data acceleration
- Supporting fast block acceleration
- Supporting ATA security
- Supporting SRAM ECC
- Supporting deep recovery mode for user data
- Supporting read-only mode for critical errors
- Supporting data stream distribution
- Supporting Pyrite 2.0

Performance

256GB

- Read: Up to 4,900MB/s
- Write: Up to 1,500MB/s

512GB

- Read: Up to 5,200MB/s
- Write: Up to 3,000MB/s
-

TBW

- 256GB: 188TB
- 512GB: 400TB

Power Consumption

- Active write: 3,300 mW (512GB)
- Active read: 3,300 mW (512GB)

Temperatures

- Operating: 0°C~70°C
- Non-operating: -40°C~85°C

Shock & Vibration

- Shock: 1,500G, duration 0.5ms, Half Sine Wave (Non-operating)
- Vibration: 10~2,000Hz, 20G, 3.08Grms, 30min/axis(X,Y,Z) (Non-operating)

MTBF

- 1,500,000 hours

UBER

- < 1 sector per 10^15 bits read

Weight

- 256GB/512GB
- Max 8g

Certification

- UNH-IOL
- PCI-SIG
- Ulink Protocol & Regression
- Intel Open Lab MS & Athena certification
- TCG Pyrite 2.0 Compliance

Power

- L1.2: 5mW

Revision History

Date	Description
April 04th, 2025	Initial Release.

Contents

1 Introduction

1.1 General Description

This document describes the specifications of XP2000 SSDs.
XP2000 SSDs use NAND Flash Memory and provide high reliability in a small form factor. It supports the PCIe 4.0 interface standard with up to four lanes, showing a much better performance than SATA SSDs.

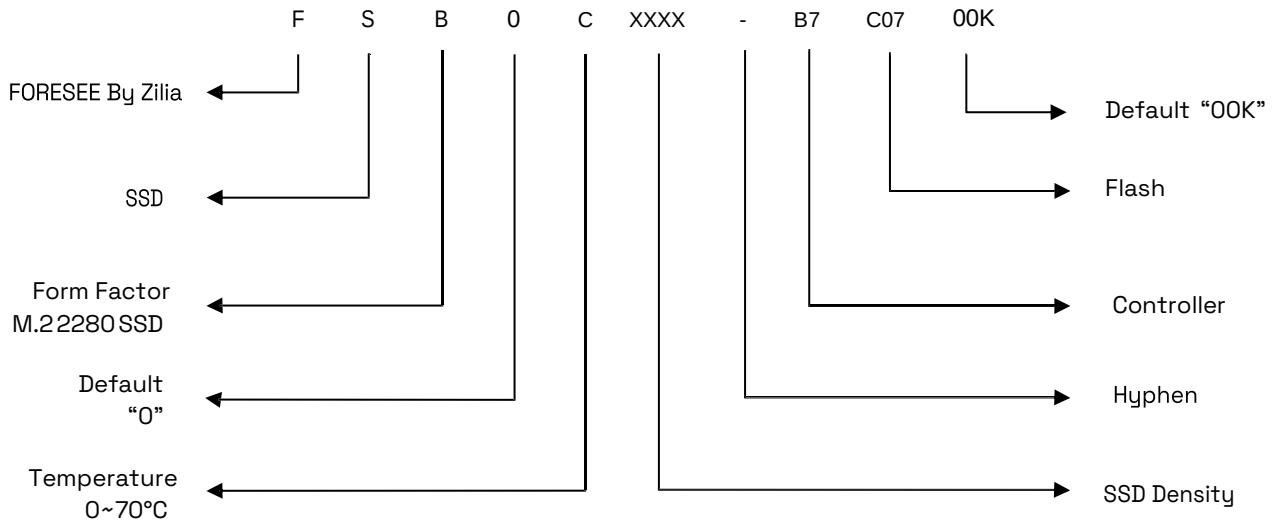
XP2000 SSDs come in different capacities: 256GB, 512GB. With four lanes, their sequential performance is up to 5,200MB/s for read operation and 3,000MB/s for write operation, and their random performance is up to 430k IOPS for read operation and 690k IOPS for write operation. They also provide rugged features, delivering a high MTBF.

1.2 Product Line-up

Table 1 Product Line-up

Type	Capacity	Model	Part Number
PCIe M.2 2280 SSD	256GB	XP2000F256G	FSB0C256G-B7C0700K
PCIe M.2 2280 SSD	512GB	XP2000F512G	FSB0C512G-B7C0700K

1.3 Ordering Information



1.4 SSD Function Block Diagram

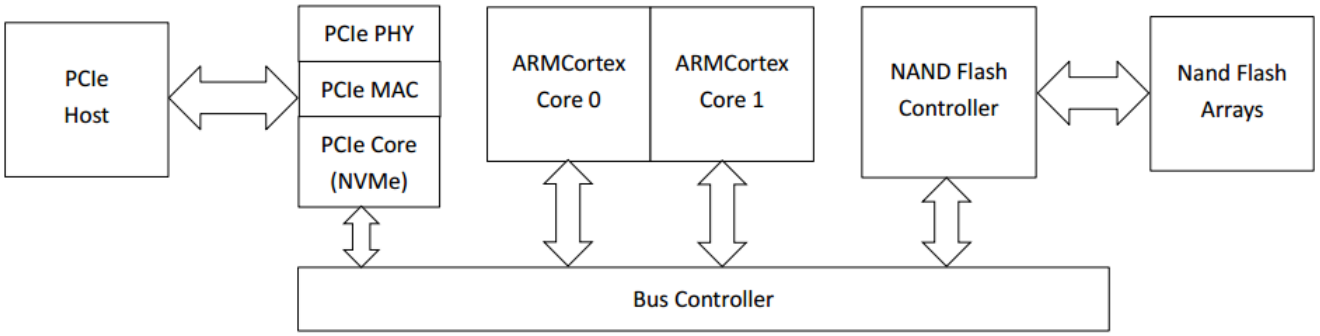


Figure 1 Function Block Diagram

2 Product Specifications

2.1 Capacity

Table 2 User-Addressable Sectors

Nominal Capacity	256GB	512GB
User-Addressable Sectors	500,118,192	1,000,215,216
Bytes per Sector	512	

Notes:

- 1 Megabyte (MB) = 1 million bytes; 1 Gigabyte (GB) = 1 billion bytes
- User-Addressable Sectors in the LBA mode is calculated by IDEMA rule.

2.2 Performance

Table 3 Drive Performance

Parameter	Unit	256GB	512GB
Sequential Read (Max)	MB/S	4,900	5,200
Sequential Write (Max)	MB/S	1,500	3,000
Random Read 4K (Max)	IOPS	220K	430K
Random Write 4K (Max)	IOPS	380K	690K

Notes:

- Performance measured using CrystalDiskMark 8.0.0 (Sequential data size, QD=8 by Thread=1 (Total QD=8). 4KB data size, QD=32 by Thread 16 (Total QD=512))
- Write cache enabled
- 1MB/sec = 1,048,576 bytes/sec was used in measuring sequential performance.
- System: Intel Z590 Chipset, Intel Core i7-11700K@3.6GHz, 8GB DDR4
- OS: Windows 10 x64 with HMB turned on

Actual performance may vary depending on use conditions and environment.

2.3 Power

Table 4 Power Consumption

Parameter		256GB	512GB
Active[1] (MaxRMS)	Read	3,200mW	3,300mW
	Write	2,500mW	3,300mW
Idle[2]		780mW	780mW
L1.2[2]		5mW	5mW

Notes:

- CPU: Intel Core i7-11700K@3.6GHz
- DRAM: 8GB DDR4
- Chipset: Intel Z590
- OS: Windows 10 x64

1. Active power is measured on sequential write and read (Test tool: CrystalDiskMark 7.0.0).
2. Idle power is measured on PS3 (L1.2 enabled) and L1.2 power is measured on PS4 (L1.2 enabled).

Table 5 Voltage Requirements

Item	Requirement
Allowable voltage	3.3V ± 5%
Allowable noise/ripple	100mV p-p or less

2.4 System Reliability

Table 6 MTBF Specifications

Capacity	MTBF
256GB	1,500,000 hours
512GB	1,500,000 hours

Note: MTBF is short for Mean Time Between Failures. The annual failure ratio is 0.4%.

Table 7 UBER Specifications

Parameter	Specification
UBER	< 1 sector per 10^15 bits read

2.5 Endurance

Table 7 Endurance Specifications

TBW	
256GB	512GB
188TB	400TB

Notes:

- TBW (Terabytes Written) is a measurement of the expected lifespan of an SSD, which represents the amount of data written to the device. To calculate the TBW of an SSD, the following equation is applied:
  TBW = [(NAND Endurance) x (SSD Capacity)] / WAF
  NAND Endurance: NAND endurance refers to the P/E (Program/Erase) cycles of a NAND flash. SSD Capacity: SSD capacity is the specific capacity in total of an SSD.
  WAF: Write Amplification Factor (WAF) is a numerical value representing the ratio between the amount of data that an SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near 1, guarantees better endurance and lower frequency of data written to flash memory.
- The above TBW values are calculated based on 256GB,WAF=1.36; 512GB,WAF=1.27 (Cilent:JESD218 test method and JESD219A workload）
- TBW may differ according to different flash configurations and platforms.
- The endurance of an SSD could be estimated based on user behaviors, NAND endurance cycles, and write amplification factors. It is not guaranteed by the flash vendor.

2.6 Environmental Specifications

Table 8 Power Consumption

Features	Operating	Non-operating
Temperatures	0°C to 70°C	-40°C to 85°C
Humidity	5% to 95%, without condensation	
Vibration	10~2000Hz, 20G, 3.08Grms, 30min/axis(X,Y,Z) (Non-operating)	
Shock	1500G, duration 0.5ms, Half Sine Wave (Non-operating)	

Notes:

- Temperature is measured by SMART Temperature. Proper airflow is recommended.
- Humidity is measured in a non-condensing environment.

3 Mechanical Specifications

Table 9 M.2 2280 SSD Physical Dimensions and Weight

Capacity	Height(mm)	Width (mm)	Length (mm)	Weight (gram)
256GB/512GB	MAX 2.23	22.00±0.15	80.00±0.15	MAX 8

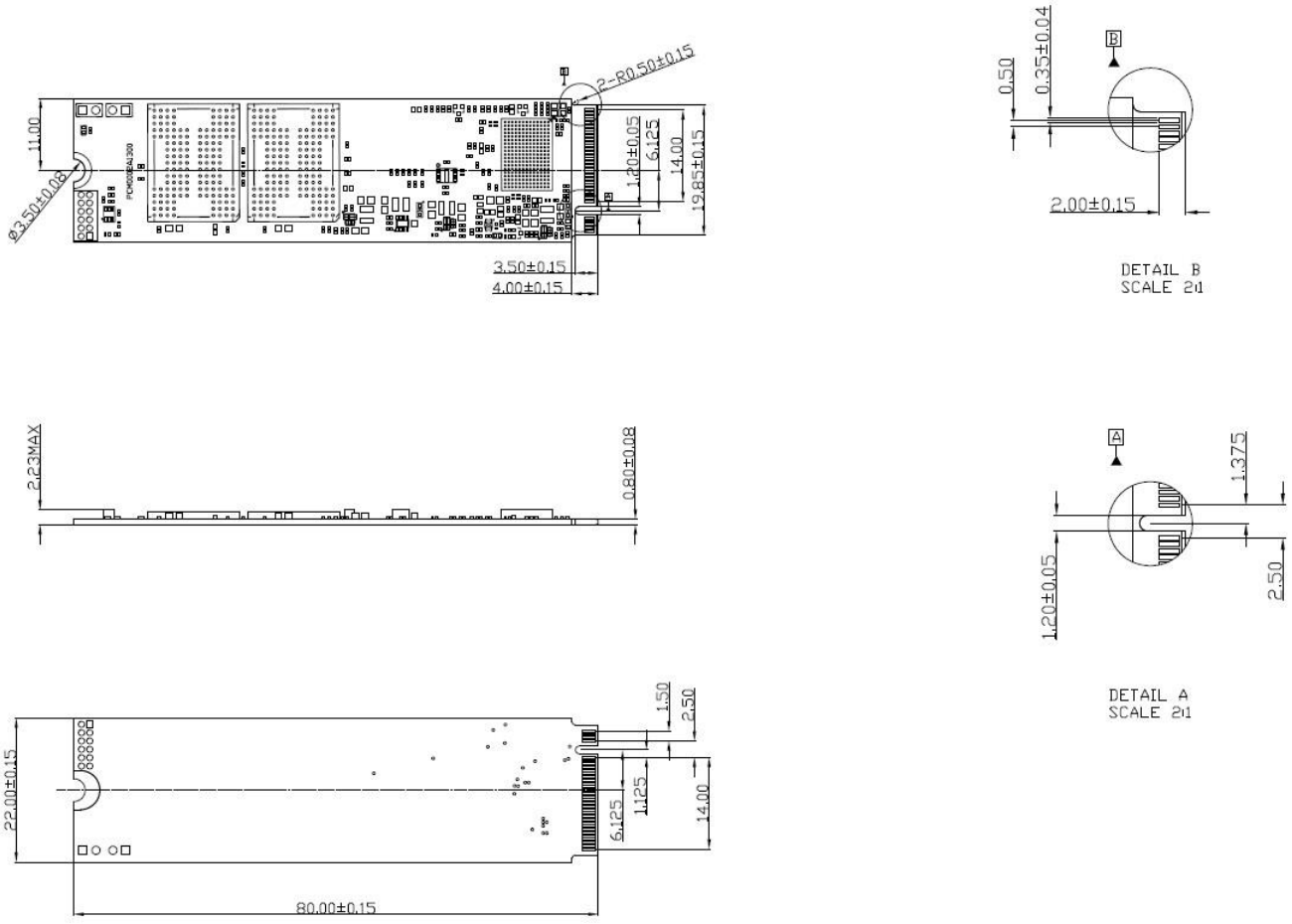


Figure 2 M.2 2280 Physical Dimension

4 Electrical Interface Specifications

4.1 Connector Pin Location

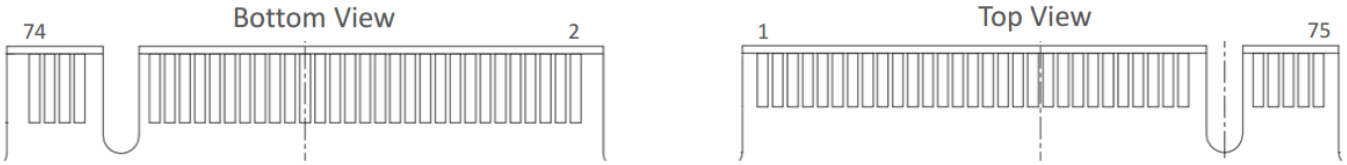


Figure 3 M.2 2280 Signal and Power pins

4.2 M.2 2280 Pin Assignments and Definition

Table 10 M.2 2280 Connector Pin Assignment

Pin #	Assignment	Description	Pin #	Assignment	Description
1	GND	Ground	2	3.3V	3.3V source
3	GND	Ground	4	3.3V	3.3V source
5	PETn3	PCIe TX	6	N/C	N/C
7	PETp3	PCIe TX	8	PLN#	Power Loss Notification
9	GND	Ground	10	LED_1#	Device Active Signal
11	PERn3	PCIe RX	12	3.3V	3.3V source
13	PERp3	PCIe RX	14	3.3V	3.3V source
15	GND	Ground	16	3.3V	3.3V source
17	PETn2	PCIe TX	18	3.3V	3.3V source
19	PETp2	PCIe TX	20	N/C	N/C
21	GND	Ground	22	N/C	N/C
23	PERn2	PCIe RX	24	N/C	N/C
25	PERp2	PCIe RX	26	N/C	N/C
27	GND	Ground	28	N/C	N/C
29	PETn1	PCIe TX	30	PLA_S3#	Power Loss Acknowledge
31	PETp1	PCIe TX	32	N/C	N/C
33	GND	Ground	34	N/C	N/C
35	PERn1	PCIe RX	36	N/C	N/C
37	PERp1	PCIe RX	38	N/C	N/C
39	GND	Ground	40	SMB_CLK	SMBus Clock
41	PETn0	PCIe TX	42	SMB_DATA	SMBus Data
43	PETp0	PCIe TX	44	N/C	N/C
45	GND	Ground	46	N/C	N/C
47	PERn0	PCIe RX	48	N/C	N/C
49	PERp0	PCIe RX	50	PERST#	PCIe Reset
51	GND	Ground	52	CLKREQ#	PCIe Device Clock Request
53	REFCLKN	PCIe Reference Clock	54	N/C	N/C
55	REFCLKP	PCIe Reference Clock	56	N/C	N/C
57	GND	Ground	58	N/C	N/C
59	N/C	Mechanical Notch	60	N/C	Mechanical Notch
61	N/C	Mechanical Notch	62	N/C	Mechanical Notch

Pin #	Assignment	Description	Pin #	Assignment	Description
63	N/C	Mechanical Notch	64	N/C	Mechanical Notch
65	N/C	Mechanical Notch	66	N/C	Mechanical Notch
67	N/C	N/C	68	N/C	N/C
69	N/C	N/C	70	3.3V	3.3V source
71	GND	Ground	72	3.3V	3.3V source
73	GND	Ground	74	3.3V	3.3V source
75	GND	Ground			

Table 11 Simple Indicator Protocol for SSD LED States (Optional)

ASPM		LED Status
Active State (Host sends CMD to SSD)		Blinking
Idle	Low Power standby	Off
Deep Sleep	Deep Sleep Power savings	Off

Note: ASPM (Active State Power Management)

5 PCI and NVM Express Configuration Registers

5.1 PCI Express Registers

5.1.1 PCI Register Summary

Table 12 PCI Register Summary

Start Address(Hex)	End Address(Hex)	Name	Type
00h	3Fh	PCI Header	PCI Configuration Header
40h	47h	PCI Power Management Capability	PCI Capability
50h	67h	MSI Capability	PCI Capability
70h	A3h	PCI Express Capability	PCI Capability
B0h	BBh	MSI-X Capability	PCI Capability
100h	12Bh	Advanced Error Reporting Capability	PCI Extended Capability
148h	15Bh	Secondary PCI Express Capability	PCI Extended Capability
168h	16Bh	Latency Tolerance Reporting Capability	PCI Extended Capability
170h	17Bh	L1 Sub-states Capability	PCI Extended Capabilty
180h	1B7h	Vendor-Specific Extended Capability	PCI Extended Capability
1B8h	1C3h	Data Link Feature Extended Capability	PCI Extended Capability

5.1.2 PCI Configuration Header Space Registers Detail

5.1.2.1 PCI Configuration Header Space Registers

Table 13 PCI Header Space Summary

Start Address(Hex)	End Address(Hex)	Symbol	Description
00h	03h	IDTF	Identifiers
04h	05h	CMD	Command Register
06h	07h	STS	Status Register
08h	08h	REVID	Revision ID
09h	0Bh	CC	Class Codes
0Ch	0Ch	CLS	Cache Line Size
0Dh	0Dh	LT	Latency Timer
0Eh	0Eh	HTYPE	Header Type
0Fh	0Fh	BIST	Built in Self Test
10h	13h	BAR0	Base Address Register 0
14h	17h	BAR1	Base Address Register 1
18h	1Bh	BAR2	Base Address Register 2
1Ch	1Fh	BAR3	Base Address Register 3
20h	23h	BAR4	Base Address Register 4
24h	27h	BAR5	Base Address Register 5
28h	2Bh	CCPTR	CardBus CIS Pointer
2Ch	2Fh	SS	Subsystem Identifiers
30h	33h	EXPROM	Expansion ROM Base

Start Address(Hex)	End Address(Hex)	Symbol	Description
34h	34h	CAP	Capabilities Pointer
35h	3Bh	R	Reserved
3Ch	3Dh	INTR	Interrupt Information
3Eh	3Eh	MGNT	Minimum Grant
3Fh	3Fh	MLAT	Maximum Latency

Table 14 Identifier Register

Bits	Type	Default Value(Hex)	Description
31:16	RO	5216h	Device ID
0:15	RO	1D97h	Vendor ID

Table 15 Command Register

Bits	Type	Default Value(Hex)	Description
15:11	RSVD	0h	Reserved
10	RW	1h	Interrupt Disable
9	RO	0h	Fast Back-to-Back Enable
8	RW	0h	SERR# Enable
7	RO	0h	IDSEL Stepping/Wait Cycle Control
6	RW	0h	Parity Error Response Enable
5	RO	0h	VGA Palette Snooping Enable
4	RO	0h	Memory Write and Invalidate Enable
3	RO	0h	Special Cycle Enable
2	RW	1h	Bus Master Enable
1	RW	1h	Memory Space Enable
0	RW	0h	I/O Space Enable

Table 16 Status Register

Bits	Type	Default Value(Hex)	Description
15	RW1C	0h	Detected Parity Error
14	RW1C	0h	Signaled System Error
13	RW1C	0h	Received Master Abort
12	RW1C	0h	Received Target Abort
11	RW1C	0h	Signaled Target Abort
10:9	RO	0h	DEVSEL Timing
8	RW1C	0h	Master Data Parity Error Detected
7	RO	0h	Fast Back-to-Back Transaction Capable
6	RO	0h	Reserved
5	RO	0h	66MHz Capable
4	RO	1h	Capabilities List

Bits	Type	Default Value(Hex)	Description
3	RO	0h	Interrupt Status
2:0	RO	0h	Reserved

Table 17 Revision ID Register

Bits	Type	Default Value(Hex)	Description
7:0	RO	1h	RevisionID

Table 18 Class Code Register

Bits	Type	Default Value(Hex)	Description
23:16	RO	01h	Base Class Code
15:8	RO	08h	Sub Class Code
7:0	RO	02h	Programming Interface

Table 19 Cache Line Size Register

Bits	Type	Default Value(Hex)	Description
7:0	RW	10h	Cache Line Size

Table 20 Master Latency Timer Register

Bits	Type	Default(Hex)	Description
7:0	RO	0h	Latency Timer

Table 21 Header Type Register

Bits	Type	Default(Hex)	Description
7	RO	0h	Multi-Function Device
6:0	RO	0h	Reserved

Table 22 Built-in Self-Test Register

Bits	Type	Default(Hex)	Description
7:0	RO	0h	BIST Capable
6	RW	0h	Start BIST
5:4	RSVD	0h	Reserved
3:0	RO	0h	Completion Code

Table 23 Memory Register Base Address Lower 32-bits (BAR0) Register

Bits	Type	Default(Hex)	Description
31:4	RW	0h	Base Address
3	RO	0h	Pre-Fetchable
2:1	RO	2h	Type
0	RO	0h	Space Indicator

Table 24 Memory Register Base Address Upper 32-bits (BAR1)

Bits	Type	Default(Hex)	Description
31:0	RW	0h	Base Address

Table 25 Index/Data Pair Register Base Address (BAR2) Register

Bits	Type	Default(Hex)	Description
31:4	RO	0h	Base Address
3	RO	0h	Pre-Fetchable
2:1	RO	0h	Type
0	RO	0h	Space Indicator

Table 26 Vendor-specific BAR3 Register

Bits	Type	Default(Hex)	Description
31:4	RO	0h	Base Address
3	RO	0h	Pre-Fetchable
2:1	RO	0h	Type
0	RO	0h	Space Indicator

Table 27 Vendor-specific BAR4 Register

Bits	Type	Default(Hex)	Description
31:4	RO	0h	Base Address
3	RO	0h	Pre-Fetchable
2:1	RO	0h	Type
0	RO	0h	Space Indicator

Table 28 Vendor-specific BAR5 Register

Bits	Type	Default(Hex)	Description
31:4	RO	0h	Base Address
3	RO	0h	Pre-Fetchable
2:1	RO	0h	Type
0	RO	0h	Space Indicator
31:0	RO	0h	N/A

Table 30 Subsystem Identifier Register

Bits	Type	Default(Hex)	Description
31:16	RO	5216h	Subsystem ID
15:0	RO	1DBEh	Subsystem Vendor ID

Table 31 Expansion ROM Register

Bits	Type	Default(Hex)	Description
31:11	RW	0h	Expansion ROM Base
10:1	RSVD	0h	Reserved
0	RW	0h	Expansion ROM

Table 32 Capabilities Pointer Register

Bits	Type	Default(Hex)	Description
7:0	RO	40h	Capability Pointer

Table 33 Interrupt Information Register

Bits	Type	Default(Hex)	Description
15:8	RO	01h	Interrupt Pin
7:0	RW	FFh	Interrupt Line

Table 34 Minimum Grant Register

Bits	Type	Default(Hex)	Description
7:0	RO	0h	Minimum Grant

Table 35 Maximum Latency Register

Bits	Type	Default(Hex)	Description
7:0	RO	0h	Maximum Latency

5.1.3 PCI Capability Registers Details

5.1.3.1 PCI Power Management Capabilities

Table 36 Summary of PCI Power Management Capabilities

Start Address(Hex)	End Address(Hex)	Symbol	Description
40h	41h	PCIPM_ID	PCI Power Management Capability
42h	42h	NEXT_Item_Ptr	Next Item Pointer
43h	43h	Cap_ID	Capability ID
44h	44h	Data	Data
45h	46h	PMCSR	Power Management Control/Status

Table 37 PCI Power Management Capability ID Register

Bits	Type	Default(Hex)	Description
15:8	RO	50h	Next Capability
7:0	RO	1h	Capability ID

Table 38 PCI Power Management Capability Register

Bits	Type	Default(Hex)	Description
15:11	RO	0h	PME Support
10	RO	0h	D2 Support
9	RO	0h	D1 Support
8:6	RO	0h	AUX Current
5	RO	0h	Device Specific Initialization
4	RO	0h	Immediate_Readiness_on_Return_to_D0
3	RO	0h	PME Clock
2:0	RO	3h	Version (Support for PCI Bus Power Management Interface

Table 39 PCI Power Management Control and Status Register

Bits	Type	Default(Hex)	Description
31:24	RO	0h	Reserved
23	RW	0h	Reserved
22	RW	0h	Reserved
21:16	RO	0h	Reserved
15	RW1C	0h	PME_Status
14:13	RO	0h	Data Scale
12:9	RW	0h	Data Select
8	RW	0h	PME enable
7:4	RO	0h	Reserved
3	RO	1h	No Soft Reset
2	RO	0h	Reserved
1:0	RW	0h	Power State

5.1.3.2 MSI Capabilities

Table 40 Summary of Message Signaled Interrupt Capabilities

Start Address(Hex)	End Address(Hex)	Symbol	Description
50h	51h	MSI_ID	Message Signaled Interrupt Capability ID
52h	53h	MSI_MC	Message Control
54h	57h	MSI_MA	Message Signaled Interrupt Message
58h	5Bh	MSI_MUA	Message Signaled Interrupt Upper Address
5Ch	5Dh	MSI_MDATA	Message Data
60h	63h	MSI_MMASK	Mask Bits
64h	67h	MSI_MPEND	Pending Bits

Table 41 Message Signaled Interrupt Capability ID Register

Bits	Type	Default(Hex)	Description
15:8	RO	70h	Next Capability
7:0	RO	05h	Capability ID

Table 42 Message Signaled Interrupt Control Register

Bits	Type	Default(Hex)	Description
15:11	RSVO	0h	Reserved
10	RW	0h	Reserved
9	RO	0h	Reserved
8	RO	1h	Per Vector Masking
7	RO	1h	64-bit Address Capable
6:4	RW	0h	Multiple Message Enable
3:1	RO	0h	Multiple Message Capable
0	RW	0h	MSI Enable

Table 43 Message Signaled Interrupt Address Register

Bits	Type	Default(Hex)	Description
31:2	RW	0h	Address
1:0	RO	0h	Reserved

Table 44 Message Signaled Interrupt Upper Address Register

Bits	Type	Default(Hex)	Description
31:0	RW	0h	Upper Address
31:16	RSVDP	0h	Reserved
15:0	RW	0h	Extended Message Data

Table 46 Message Signaled Interrupt Mask Bits Register

Bits	Type	Default(Hex)	Description
31:0	RW	0h	Mask Bits

Table 47 Message Signaled Interrupt Pending Bits Register

Bits	Type	Default(Hex)	Description
31:0	RO	0h	Pending Bits

5.1.3.3 PCI Express Capabilities

Table 48 Summary of PCI Express Capabilities

Start Address(Hex)	End Address(Hex)	Symbol	Description
70h	71h	PCIE_ID	PCI Express Capability ID
72h	73h	PCIE_CAP	PCI Express Capabilities
74h	77h	PCIE_DCAP	PCI Express Device Capabilities
78h	79h	PCIE_DC	PCI Express Device Control
7Ah	7Bh	PCIE_DS	PCI Express Device Status
7Ch	7Fh	PCIE_LCAP	PCI Express Link Capabilities
80h	81h	PCIE_LC	PCI Express Link Control
82h	83h	PCIE_LS	PCI Express Link Status
84h	87h	Slot Capabilities Register	Reserved
88h	89h	Slot Control Register	Reserved
8Ah	8Bh	Slot Status Register	Reserved
8Ch	8Dh	Root Control Register	Reserved
8Eh	8Fh	Root Capabilities Register	Reserved
90h	93h	Root Status Register	Reserved
94h	97h	PCIE_DCAP2	PCI Express Device Capabilities 2
98h	99h	PCIE_DC2	PCI Express Device Control 2
9Ah	9Bh	PCIE_DS2	PCI Express Device Status 2
9Ch	9Fh	PCIE_LCAP2	PCI Express Link Capabilities 2
A0h	A1h	PCIE_LC2	
A2h	A3h	PCIE_LS2	PCI Express Link Status 2

Table 49 PCI Express Capability ID Register

Bits	Type	Default(Hex)	Description
15:8	RO	B0h	Next Pointer
7:0	RO	10h	Capability ID

Table 50 PCI Express Capability Register

Bits	Type	Default(Hex)	Description
15	RsvdP	0h	Reserved
14	RsvdP	0h	Undefined
13:9	RO	0h	Interrupt Message
8	HwInit	0h	Slot Implementation
7:4	RO	0h	Device/Port Type
3:0	RO	2h	Capability Version

Table 51 PCI Express Device Capability Register

Bits	Type	Default(Hex)	Description
31:29	RsvdP	0h	Reserved
28	RO	1h	Function Level Reset Capability
27:26	RO	1h	Captured Slot Power Limit Scale
25:18	RO	FAh	Captured Slot Power Limit Value
17:16	RsvdP	0h	Reserved
15	RO	1h	Role-based Error Reporting
14:12	RsvdP	0h	Reserved
11:9	RO	7h	Endpoint L1 Acceptable Latency
8:6	RO	7h	Endpoint L0 Acceptable Latency
5	RO	0h	Extended Tag Field Supported
4:3	RO	0h	Phantom Functions Supported
2:0	RO	2h	Max Payload Size Supported

Table 52 PCI Express Device Control Register

Bits	Type	Default(Hex)	Description
15	RW	0h	Initiate Function Level Reset
14:12	RW	2h	Max Read Request Size
11	RW	0h	Enable No Snoop
10	RWS	0h	Aux Power PM Enable
9	RW	0h	Phantom Functions Enable
8	RW	0h	Extended Tag Enable
7:5	RW	1h	Max Payload Size
4	RW	1h	Enable Relaxed Ordering
3	RW	0h	Unsupported Request Reporting Enable

Bits	Type	Default(Hex)	Description
2	RW	0h	Fatal Error Reporting Enable
1	RW	0h	Non-Fatal Error Reporting Enable
0	RW	0h	Correctable Error Reporting Enable

Table 53 PCI Express Device Status Register

Bits	Type	Default(Hex)	Description
15:6	RsvdZ	0h	Reserved
5	RO	0h	TransactionsPending
4	RO	1h	Aux Power Detected
3	RW1C	0h	Unsupported Request Detected
2	RW1C	0h	Fatal Error Detected
1	RW1C	0h	Non-Fatal Error Detected
0	RW1C	0h	Correctable Error Detected

Table 54 PCI Express Link Capability Register

Bits	Type	Default(Hex)	Description
31:24	HwInit	0h (Port 0)	Port Number
23	RsvdP	0h	Reserved
22	HwInit	1h	ASPM Optionality Compliance
21	RO	0h	Link Bandwidth Notification Capability
20	RO	0h	Data Link Layer Link Active Reporting Capable
19	RO	0h	Surprise Down Error Reporting Capable
18	RO	0h	Clock Power Management
17:15	RO	6h	L1 Exit Latency
14:12	RO	3h	L0s Exit Latency
11:10	RO	2h	Active State Power Management Support
9:4	RO	4h (x4 link)	Maximum Link Width
3:0	RO	3h	Max Link Speeds

Table 55 PCI Express Link Control Register

Bits	Type	Default Value(Hex)	Description
15:10	RsvdP	0h	Reserved
9	RW	0h	Hardware Autonomous Width Disable
8	RW	0h	Enable Clock Power Management
7	RW	0h	Extended Sync
6	RW	1h	Common Clock Configuration
5	RsvdP	0h	Reserved
4	RsvdP	0h	Reserved
3	RW	0h	Read Completion Boundary

Bits	Type	Default Value(Hex)	Description
2	RsvdP	0h	Reserved
1:0	RW	0h	Active State Power Management Control

Table 56 PCI Express Link Status Register

Bits	Type	Default Value(Hex)	Description
15:13	RO	0h	Reserved
12	HwInit	1h	Slot Clock Configuration
11:10	RO	0h	Reserved
9:4	RO	4h	Negotiated Link Width
3:0	RO	3h	Current Link Speed

Table 57 PCI Express Device Capability 2 Register

Bits	Type	Default Value(Hex)	Description
31:24	RO	0h	Reserved
23:22	RsvdP	0h	Max End-End TLP Prefixes
21	HwInit	0h	End-End TLP Prefix Supported
20	RO	0h	Extended Format Field Supported
19:18	HwInit	0h	OBFF Supported
17	HwInit	0h	10-Bit Tag Requester Supported
16	HwInit	0h	10-Bit Tag Completer Supported
15:14	RO	0h	LN System CLS
13:12	HwInit	0h	TPH Completer Supported
11	RO	1h	Latency Tolerance Reporting Supported
10	HwInit	0h	No RO-enabled PR-PR Passing
9	RO	0h	128-bit CAS Completer Supported
8	RO	0h	64-bit Atomic Op Completer Supported
7	RO	0h	32-bit Atomic Op Completer Supported
6	RO	0h	Atomic Op Routing Supported
5	RO	0h	ARI Forwarding Supported
4	RO	1h	Completion Timeout Disable Supported
3:0	HwInit	Fh	Completion Timeout Ranges Supported

Table 58 PCI Express Device Control 2 Register

Bits	Type	Default Value(Hex)	Description
31:15	RO	0h	Reserved
14:13	RW	0h	OBFF Enable
12:11	RO	0h	Reserved
10	RW	1h	Latency Tolerance Reporting Mechanism Enable
9:5	RO	0h	Reserved
4	RW	0h	Completion Timeout Disable
3:0	RW	Eh	Completion Timeout Value

Table 59 PCI Express Device Status 2 Register

Bits	Type	Default Value(Hex)	Description
15:0	RsvdZ	0h	Reserved

Table 60 PCI Express Link Capability 2 Register

Bits	Type	Default Value(Hex)	Description
31	RO	0h	DRS supported
30:25	RsvdP	0h	Reserved
24	RsvdP	0h	Two Retimers Presence Detect Supported
23	HWinit	0h	Retimer Presence Detect Supported
22:16	HWinit	0h	Lower SKP OS Reception Supported Speed Vector
15:9	HWinit	0h	Lower SKP OS Generation Supported Speed Vector
8	RO	0h	Cross-Link Supported
7:1	HWinit	7h	Supported Speeds Vector
0	RsvdP	0h	Reserved

Table 61 PCI Express Link Control 2 Register

Bits	Type	Default Value(Hex)	Description
15:12	RWS	0h	Compliance De-emphasis
11	RWS	0h	Compliance SOS
10	RWS	0h	Enter Modified Compliance
9:7	RWS	0h	TransmitMargin
6	HwInit	0h	Selectable De-Emphasis
5	RWS	0h	Hardware Autonomous Speed Disable
4	RWS	0h	Enter Compliance
3:0	RWS	3h	Target Link Speed

Table 1 PCI Express Link Status 2 Register

Bits	Type	Default Value(Hex)	Description
15:6	RSVDZ	0h	Reserved
5	RW1CS	0h	Link Equalization Request 16.0GT/s
4	ROS	1h	Equalization 16.0GT/s Phase 3 Successful
3	ROS	1h	Equalization 16.0GT/s Phase 2 Successful
2	ROS	1h	Equalization 16.0GT/s Phase 1 Successful
1	ROS	1h	Equalization 16.0GT/s Complete
0	RO	0h	Current De-Emphasis

5.1.3.4 MSI-X Capabilities

Table 63 Summary of MSI-X Capabilities

Start Address(Hex)	End Address(Hex)	Symbol	Description
B0h	B1h	MSIX_ID	MSI-X Capability ID
B2h	B3h	MSIX_CAP	MSI-X Message Control
B4h	B7h	MSIX_TBL	MSI-X Table Offset and Table
B8h	B8h	MSIX_PBA	MSI-X PBA Offset and PBA BIR

Table 64 MSI-X Identifier Register

Bits	Type	Default Value(Hex)	Description
15:8	RO	00h	Next Capability
7:0	RO	11h	Capability ID

Table 65 MSI-X Control Register

Bits	Type	Default Value(Hex)	Description
15	RW	1h	MSI-X Enable
14	RW	0h	Function Mask
13:11	Rsvd	0h	Reserved
10:0	RO	8h	Table Size

Table 66 MSI-X Table Offset Register

Bits	Type	Default Value(Hex)	Description
31:3	RO	400h	Table Offset
2:0	RO	0h	Table BIR

Table 2 MSI-X Pending Bit Array Offset Register

Bits	Type	Default Value(Hex)	Description
31:3	RO	600h	Pending Bit Array Offset
2:0	RO	0h	Pending Bit Array BIR

5.1.4 PCI Extended Capability Details

5.1.4.1 Advanced Error Reporting Capabilities

Table 68 Summary of Advanced Error Reporting Capabilities

Start Address(Hex)	End Address(Hex)	Symbol	Description
100h	103h	AER_ID	AER Capability ID
104h	107h	AER_UCES	AER Uncorrectable Error Status
108h	10Bh	AER_UCEM	AER Uncorrectable Error Mask
10Ch	10Fh	AER_UCESEV	AER Uncorrectable Error Severity
110h	113h	AER_CES	AER Correctable Error Status
114h	117h	AER_CEM	AER Correctable Error Mask
118h	11Bh	AER_CC	AER Advanced Error Capabilities and Control
11Ch	12Bh	AER_HL	AER Header Log

Table 69 AER Capability ID Register

Bits	Type	Default Value(Hex)	Description
31:20	RO	148h	Next Pointer (Points to Alternative Routing-ID Capability Header Offset)
19:16	RO	2h	Capability Version
15:0	RO	1h	Capability ID

Table 70 AER Uncorrectable Error Status Register

Bits	Type	Default Value(Hex)	Description
31:27	RsvdZ	0h	Reserved
26	RW1CS	0h	Poisoned TLP Egress Blocked Status
25	RW1CS	0h	Capability ID
24	RW1CS	0h	Atomic Op Egress Blocked Status
23	RW1CS	0h	MC Blocked TLP Status
22	RW1CS	0h	Uncorrectable Internal Error Status
21	RW1CS	0h	ACS Violation Status
20	RW1CS	0h	Unsupported Request Error Status
19	RW1CS	0h	ECRC Error Status
18	RW1CS	0h	Malformed TLP Status
17	RW1CS	0h	Receiver Overflow Status
16	RW1CS	0h	Unexpected Completion Status

Bits	Type	Default Value(Hex)	Description
15	RW1CS	0h	Completer Abort Status
14	RW1CS	0h	Completion Timeout Status
13	RW1CS	0h	Flow Control Protocol Error Status
12	RW1CS	0h	Poisoned TLP Status
11:6	RsvdZ	0h	Reserved
5	RW1CS	0h	Surprise Down Error Status
4	RW1CS	0h	Data Link Protocol Error Status
3:1	RsvdZ	0h	Reserved
0	Undefined	0h	Undefined

Table 71 AER Uncorrectable Error Mask Register

Bits	Type	Default Value(Hex)	Description
31:26	RsvdZ	0h	Reserved
25	RWS	0h	TLP Prefix Blocked Error Mask
24	RWS	0h	Atomic Op Egress Blocked Mask
23	RWS	0h	MC Blocked TLP Mask
22	RWS	1h	Uncorrectable Internal Error Mask
21	RWS	0h	ACS Violation Mask
20	RWS	0h	Unsupported Request Error Mask
19	RWS	0h	ECRC Error Mask
18	RWS	0h	Malformed TLP Mask
17	RWS	0h	Receiver Overflow Mask
16	RWS	0h	Unexpected Completion Mask
15	RWS	0h	Completer Abort Mask
14	RWS	0h	Completion Timeout Mask
13	RWS	0h	Flow Control Protocol Error Mask
12	RWS	0h	Poisoned TLP Mask
11:6	RsvdZ	0h	Reserved
5	RWS	0h	Surprise Down Error Mask
4	RWS	0h	Data Link Protocol Error Mask
3:1	RsvdZ	0h	Reserved
0	Undefined	0h	Undefined

Table 72 AER Uncorrectable Error Severity Register

Bits	Type	Default Value(Hex)	Description
31:27	RsvdP	0h	Reserved
26	RWS	0h	Poisoned TLP Egress Blocked Severity

Bits	Type	Default Value(Hex)	Description
25	RWS	0h	TLP Prefix Blocked Error Severity
24	RWS	0h	Atomic Op Egress Blocked Severity
23	RWS	0h	MC Blocked TLP Severity
22	RWS	1h	UncorrectableInternalErrorSeverity
21	RWS	0h	ACS Violation Severity
20	RWS	0h	Unsupported Request Error Severity
19	RWS	0h	ECRC Error Severity
18	RWS	1h	Malformed TLP Severity
17	RWS	1h	ReceiverOverflowSeverity
16	RWS	0h	Unexpected Completion Severity
15	RWS	0h	Completer Abort Severity
14	RWS	0h	Completion Timeout Severity
13	RWS	1h	Flow Control Protocol Error Severity
12	RWS	0h	Poisoned TLP Severity
11:6	RsvdP	0h	Reserved
5	RWS	1h	Surprise Down Error Severity
4	RWS	1h	Data Link Protocol Error Severity
3:1	RsvdP	0h	Reserved
0	Undefined	0h	Undefined

Table 73 AER Correctable Error Status Register

Bits	Type	Default Value(Hex)	Description
31:16	RsvdZ	0h	Reserved
15	RW1CS	0h	Header Log Overflow Status
14	RW1CS	0h	Corrected Internal Error Status
13	RW1CS	0h	Advisory Non-Fatal Error Status
12	RW1CS	0h	Replay Timer Timeout Status
11:9	RsvdZ	0h	Reserved
8	RW1CS	0h	Replay Number Rollover Status
7	RW1CS	0h	Bad DLLP Status
6	RW1CS	0h	Bad TLP Status
5:1	RsvdZ	0h	Reserved
0	RW1CS	0h	Received Error Status

Table 74 AER Correctable Error Mask Register

Bits	Type	Default Value(Hex)	Description
31:16	RsvdP	0h	Reserved
15	RWS	1h	Header Log Overflow Mask

Bits	Type	Default Value(Hex)	Description
14	RWS	1h	Corrected Internal Error Mask
13	RWS	1h	Advisory Non-Fatal Error Mask
12	RWS	1h	Replay Timer Timeout Mask
11:9	RsvdP	0h	Reserved
8	RWS	0h	Replay Number Rollover Mask
7	RWS	0h	Bad DLLP Mask
6	RWS	0h	Bad TLP Mask
5:1	RsvdP	0h	Reserved
0	RWS	0h	Received Error Mask

Table 75 AER Capabilities and Control Register

Bits	Type	Default Value(Hex)	Description
31:11	RsvdP	0h	Reserved
10	RWS	0h	Multiple Header Recording Enable
9	RO	0h	Multiple Header Recording Capable
8	RWS	0h	ECRC Check Enable
7	RO	1h	ECRC Check Capable
6	RWS	0h	ECRC Generation Enable
5	RO	1h	ECRC Generation Capable
4:0	ROS	0h	First Error Pointer

Table 76 AER Header Log Register

Bits	Type	Default Value(Hex)	Description
127:120	ROS	0h	Header Byte 0
119:112	ROS	0h	Header Byte 1
111:104	ROS	0h	Header Byte 2
103:96	ROS	0h	Header Byte 3
95:88	ROS	0h	Header Byte 4
87:80	ROS	0h	Header Byte 5
79:72	ROS	0h	Header Byte 6
71:64	ROS	0h	Header Byte 7
63:56	ROS	0h	Header Byte 8
55:48	ROS	0h	Header Byte 9
47:40	ROS	0h	Header Byte 10
39:32	ROS	0h	Header Byte 11
31:24	ROS	0h	Header Byte 12
23:16	ROS	0h	Header Byte 13
15:8	ROS	0h	Header Byte 14

Bits	Type	Default Value(Hex)	Description
7:0	ROS	0h	Header Byte 15

5.1.4.2 Secondary PCI Express Capabilities

Table 77 Summary of Secondary PCI Express Capabilities

Start Address(Hex)	End Address(Hex)	Symbol	Description
148h	14Bh	SPE_ID	Secondary PCI Express Capability
14Ch	14Fh	PCIE_LC3	PCI Express Link Control 3
150h	153h	PCIE_LE	PCI Express Lane Error Status
154h	155h	PCIE_L0EC	PCI Express Lane 0 Equalization Control
156h	157h	PCIE_L1EC	PCI Express Lane 1 Equalization Control
158h	159h	PCIE_L2EC	PCI Express Lane 2 Equalization Control
15Ah	15Bh	PCIE_L3EC	PCI Express Lane 3 Equalization Control
11Ch	12Bh	AER_HL	AER Header Log

Table 78 Secondary PCI Express Capability ID Register

Bits	Type	Default Value(Hex)	Description
31:20	RO	168h	Next Pointer (Points to Physical Layer 16.0 GT/s Capability Header_Offset)
19:16	RO	1h	Capability Version
15:0	RO	19h	Capability ID (Secondary PCI Express Extended capability)

Table 79 PCI Express Link Control 3 Register

Bits	Type	Default Value(Hex)	Description
31:16	RsvdP	0h	Reserved
15:9	RW	0h	Enable Lower SKP OS Generation Vector
8:2	RsvdP	0h	Reserved
1	RW	0h	Link Equalization Request Interrupt Enable
0	RW	0h	Perform Equalization

Table 80 PCI Express Lane Error Status Register

Bits	Type	Default Value(Hex)	Description
31:4	Rsvdz	0h	Reserved
3:0	RW1CS	0h	Lane Error Status Bits

Table 3 Lane 0 Equalization Control Register

Bits	Type	Default Value(Hex)	Description
15	RsvdP	0h	Reserved
14:12	HwInit/RO	2h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	7h	Upstream Port 8.0T/s Transmitter Preset
7	RsvdP	0h	Reserved
6:4	HwInit	0h	Downstream Port 8.0T/s Receiver Preset Hint
3:0	HwInit	0h	Downstream Port 8.0T/s Transmitter Preset

Table 82 Lane 1 Equalization Control Register

Bits	Type	Default Value(Hex)	Description
15	RsvdP	0h	Reserved
14:12	HwInit/RO	11.2h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	15.7h	Upstream Port 8.0T/s Transmitter Preset
7	RsvdP	19.0h	Reserved
6:4	HwInit	23.0h	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit	27.0h	Downstream Port 8.0T/s Transmitter Preset (N/A)

Table 83 Lane 2 Equalization Control Register

Bits	Type	Default Value(Hex)	Description
15	RsvdP	0h	Reserved
14:12	HwInit/RO	2h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	7h	Upstream Port 8.0T/s Transmitter Preset
7	RsvdP	0h	Reserved
6:4	HwInit	0h	Downstream Port 8.0T/s Receiver Preset Hint
3:0	HwInit	0h	Downstream Port 8.0T/s Transmitter Preset

Table 4 Lane 3 Equalization Control Register

Bits	Type	Default Value(Hex)	Description
15	RsvdP	0h	Reserved
14:12	HwInit/RO	2h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	7h	Upstream Port 8.0T/s Transmitter Preset
7	RsvdP	0h	Reserved
6:4	HwInit	0h	Downstream Port 8.0T/s Receiver Preset Hint
3:0	HwInit	0h	Downstream Port 8.0T/s Transmitter Preset

5.1.4.3 Latency Tolerance Reporting Capability Registers

Table 85 Summary of Latency Tolerance Reporting Capabilities

Start Address(Hex)	End Address(Hex)	Symbol	Description
168h	16Bh	LTR_ID	Latency Tolerance Reporting (LTR) Capability
16Ch	16Dh	LTR_SLR	LTR Max Snoop Latency Register
16Eh	16Fh	LTR_NSLR	LTR Max No-Snoop Latency Register

Table 86 LTR Extended Capability Header

Bits	Type	Default Value(Hex)	Description
31:20	RO	170h	Next Capability Offset (Points to L1 Substates Extended Capability Header Offset)
19:16	RO	1h	Capability Version
15:0	RO	18h	PCI Express Extended Capability ID (Latency Tolerance Reporting Capability)

Table 87 LTR Max Snoop Latency Register

Bits	Type	Default Value(Hex)	Description
15:13	RsvdP	0h	Reserved
12:10	RW	2h	Max Snoop latency Scale
9:0	RW	46h	Max Snoop latency Value

Table 5 LTR Max No Snoop Latency Register

Bits	Type	Default Value(Hex)	Description
15:13	RsvdP	0h	Reserved
12:10	RW	2h	Max No Snoop Latency Scale
9:0	RW	46h	Max No Snoop Latency Value

5.1.4.4 L1 PM Substate Extended Capabilities

Table 89 L1 Substate Capability Summary

Start Address(Hex)	End Address(Hex)	Symbol	Description
170h	173h	L1S_CID	L1 Substate Capability ID
174h	177h	L1S_CR	L1 Substate Capability Register
178h	17Bh	L1S_C1R	L1 Substate Control 1 Register
17Ch	17Fh	L1S_C2R	L1 Substate Control 2 Register

Table 90 L1 Substate Extended Capability Header

Bits	Type	Default Value(Hex)	Description
31:20	RO	180h	Next Capability Offset (Points to Data Link Feature Extended Capability Header Offset)
19:16	RO	1h	Capability Version
15:0	RO	1Eh	PCI Express Extended Capability ID (L1 Substate Extended

Table 91 L1 Substate Capability Register

Bits	Type	Default Value(Hex)	Description
31:24	RsvdP	0h	Reserved
23:19	HwInit	5h	Port Power on value
18	RsvdP	0h	Reserved
17:16	HwInit	0h	Port T_Power_on scale
15:8	HwInit	Ah	Port Common_mode_restore_time
7:5	RsvdP	0h	Reserved
4	HwInit	1h	L1 PM Substates Supported
3	HwInit	1h	ASPM PM L1.1 Supported
2	HwInit	1h	ASPM PM L1.2 Supported
1	HwInit	0h	PCI PM L1.1 Supported
0	HwInit	1h	PCI PM L1.2 Supported

Table 92 L1 Substate Control 1 Register

Bits	Type	Default Value(Hex)	Description
31:29	RW	0h	LTR L1.2 Threshold Scale
28:26	RsvdP	0h	Reserved

Bits	Type	Default Value(Hex)	Description
25:16	RW	0h	LTR L1.2 Threshold value
15:8	RsvdP	0h	Common_mode_restore_tim
7:4	RsvdP	0h	Reserved
3	RW	0h	ASPM PM L1.1 Enable
2	RW	0h	ASPM PM L1.2 Enable
1	RW	0h	PCI PM L1.1 Enable
0	RW	0h	PCI PM L1.2 Enable

Table 93 L1 Substate Control 2 Register

Bits	Type	Default Value(Hex)	Description
31:8	RsvdP	0h	Reserved
7:3	RW	5h	T_POWER_ON Value
2	RsvdP	0h	Reserved
1:0	RW	0h	T_POWER_ON Scale

5.1.4.5 Vendor-specific Extended Capabilities

Table 94 Summary of Vendor-specific Extended Capabilities

Start Address(Hex)	End Address(Hex)	Description
180h	183h	Vendor-specific Extended Capability Header
184h	187h	Vendor-specific Header
188h	1B7h	VS Register

Table 95 Vendor-specific Extended Capability Header

Bits	Type	Default Value(Hex)	Description
31:20	RO	1B8h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	Bh	PCI Express Extended Capability ID (Data Link Feature Extended Capability)

Table 96 Vendor-specific Header

Bits	Type	Default Value(Hex)	Description
31:20	RO	38h	VSEC Length
19:16	RO	1h	VSEC Rev
15:0	RO	1h	VSEC ID

5.1.4.6 Vendor-specific Extended Capabilities

Table 97 Summary of Data Link Feature Extended Capabilities

Start Address(Hex	End Address(Hex)	Symbol	Description
1B8h	1BBh	DL_EXT_CAP	Data Link Feature Extended Capability
1BCh	1BFh	DL_FEA_CAP	Data Link Feature Capabilities Register
1C0h	1C3h	Remote Data Link Feature Supported	Remote Data Link Feature Supported

Table 98 Data Link Feature Extended Capability Header

Bits	Type	Default Value(Hex)	Description
31:20	RO	0h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	25h	PCI Express Extended Capability ID (Data Link Feature Extended Capability)

Table 99 Data Link Feature Capabilities Register

Bits	Type	Default Value(Hex)	Description
31	HwInit	1h	Data Link Feature Exchange Enable
30:23	RsvdP	0h	Reserved
22:0	HwInit	1h	Local Scaled Flow Control Supported

Table 100 Remote Data Link Feature Supported

Bits	Type	Default Value(Hex)	Description
31	RO	0h	Remote Data Link Feature Supported Valid
30:23	RsvdP	0h	Reserved
22:0	RO	0h	Alternate Protocol Count

5.2 NVM Express Registers

5.2.1 Register Summary

Table 101 Register Summary

Start Address(Hex)	End Address(Hex)	Name	Type
00h	07h	CAP	Controller Capabilities
08h	0Bh	VS	Version
0Ch	0Fh	INTMS	Interrupt Mask Set
10h	13h	INTMC	Interrupt Mask Clear
14h	17h	CC	ControllerConfiguration
18h	1Bh	Reserved	Reserved
1Ch	1Fh	CSTS	Controller Status
20h	23h	NSSR	NVM Subsystem Reset

Start Address(Hex)	End Address(Hex)	Name	Type
24h	27h	AQA	Admin Queue Attributes
28h	2Fh	ASQ	Admin Submission Queue Base Address
30h	37h	ACQ	Admin Completion Queue Base Address
38h	3Bh	CMBLOC	Controller Memory Buffer Location
3Ch	3Fh	CMBSZ	Controller Memory Buffer Size (Optional)
40h	43h	BPINFO	NVMe BPINFO register
44h	47h	BPRSEL	NVMe BPRSEL register
48h	4Bh	VS_IDIR_ADDR	NVMe VS Idir Addr Register
4Ch	4Fh	VS_IDIR_DATA	NVMe VS Idir Data Register

5.2.2 Controller Registers

Table 102 Controller Capabilities

Bits	Type	Name	Default Value(Hex)	Description
63:58	RO		0h	Reserved
57	RO	CMBS	0h	Controller Memory Buffer Supported
56	RO	PMRS	0h	Persistent Memory Region Supported
55:52	RO	MPSMAX	1h	Memory Page Size Maximum (Maximum is 4KB)
51:48	RO	MPSMIN	0h	Memory Page Size Minimum (Minimum is 4KB)
47:46	RO		0h	Reserved
45	RO	BPS	0h	Boot Parition Support
44:37	RO	CSS	1h	Command Sets Supported 1h: NVM command set
36	RO	NSSRS	1h	NVM Subsystem Reset Supported
35:32	RO	DSTRD	0h	Doorbell Stride 0: Stride of 4 bytes
31:24	RO	TO	F0h	Timeout 28h: 20 seconds
23:19	RO		0h	Reserved
18:17	RO	AMS	0h	Arbitration Mechanism Supported (Weighted Round Robin with Urgent supported)
16	RO	CQR	1h	Contiguous Queues Required
15:0	RO	MQES	Ffh	Maximum Queue Entries Supported (16384 entries supported)

Table 103 Version

Bits	Type	Name	Default Value(Hex)	Description
31:16	RO	MJR	1h	Major Version Number
15:8	RO	MNR	4h	Minor Version Number
7:0	RO	RSV/TER	0h	Reserved /Tertiary Version Number

Table 104 Interrupt Mask Set

Bits	Type	Name	Default Value(Hex)	Description
31:0	RWS	IVMS	0h	Interrupt Vector Mask Set

Table 105 Interrupt Mask Clear

Bits	Type	Name	Default Value(Hex)	Description
31:0	RWC	IVMC	0h	Interrupt Vector Mask Clear

Table 106 Controller Configuration

Bits	Type	Name	Default Value(Hex)	Description
31:24	RO	-	0h	Reserved
23:20	RW/RO	IOCQES	4h	I/O Completion Queue Entry Size (Configured as a power of 2) (Should be set to 4 for a 16 byte entry size)
19:16	RW/RO	IOSQES	6h	I/O Submission Queue Entry Size (Configured as a power of 2) (Should be set to 6 for a 64 byte entry size)
15:14	RW	SHN	0h	Shutdown Notification 0h: No notification 1h: Normal shutdown notification 2h: Abrupt shutdown notification 3h: Reserved CSTS.SHST indicates shutdown status.
13:11	RW	AMS	0h	Arbitration Mechanism Selected 0h: Round Robin No other values supported.
10:7	RW	MPS	0h	Memory Page Size MPS is 2^(12+MPS) Shall be within CAP.MPSMAX and CAP.MPSMIN ranges.
6:4	RW	CSS	0h	Command Set Selected 0h: NVM Command Set No other values supported
3:1	RO	-	0h	Reserved
0	RW	EN	1h	Enable When set to 1, controller shall process commands. When cleared to 0, controller shall not process commands. This field is subject to CSTS.RDY and CAP.TO restrictions.

Table 107 Controller Status

Bits	Type	Name	Default Value(Hex)	Description
31:6	RO	RSV	0h	Reserved
4	RW1C	NSSRO	0h	NVM Subsystem Reset Occurred
3:2	RO	SHST	0h	Shutdown Status 0h: Normal operation, no shutdown requested 1h: Shutdown processing occurring 2h: Shutdown processing complete 3h: Reserved
1	RO	CFS	0h	Controller Fatal Status
0	RO	RDY	1h	1h: Controller ready to process commands 0h: Controller shall not

Table 108 NVM Subsystem Reset

Bits	Type	Name	Default Value(Hex)	Description
31:0	RW	NSSRC	0h	NVM Subsystem Reset Control

Table 109 Admin Queue Attributes

Bits	Type	Name	Default Value(Hex)	Description
31:28	RO	-	0h	Reserved
27:16	RW	ACQS	7fh	Admin Completion Queue Size Max: 4096 (Value of 4095h - 0's based value)
15:12	RO	-	0h	Reserved
11:0	RW	ASQS	7fh	Admin Submission Queue Size Max: 4096 (Value of 4095h - 0's based value)

Table 110 Admin Submission Queue Base Address

Bits	Type	Name	Default Value(Hex)	Description
63:12	RW	ASQB	23F00h	Admin Submission Queue Base Address
11:0	RO	-	0h	Reserved

Table 111 Admin Completion Queue Base Address

Bits	Type	Name	Default Value(Hex)	Description
63:12	RW	ACQB	23FC00h	Admin Completion Queue Base Address
11:0	RO	-	0h	Reserved

Table 112 Controller Memory Buffer Location

Bits	Type	Name	Default Value(Hex)	Description
31:12	RO	OFST	0h	Offset

Bits	Type	Name	Default Value(Hex)	Description
11:9	RO		0h	Reserved
2:0	RO	BIR	0h	Base Indicator Register

Table 113 Controller Memory Buffer Size

Bits	Type	Name	Default Value(Hex)	Description
31:12	RO	SZ	0h	Size
11:8	RO	SZU	0h	Size Units
7:5	RO		0h	Reserved
4	RO	WDS	0h	Write Data Support
3	RO	RDS	0h	Read Data Support
2	RO	LISTS	0h	PRP SGL List Support
1	RO	CQS	0h	Completion Queue Support
0	RO	SQS	0h	Submission Queue Support

6 Supported Command Sets

6.1 Admin Command Set

The admin command set is the commands that are submitted to the Admin Submission Queues. The detailed specifications are described in the NVM Express specification document.

Table 114 Opcode for Admin Commands

Opcode (Hex)	Command Name
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Feature
0Ah	Get Feature
0Ch	Asynchronous Event Request
10h	FirmwareActivate
11h	Firmware Image Download
14h	DeviceSelf-test
80h	Format NVM
81h	Security Send
82h	Security Receive
C0h – FFh	Vendor Specific

6.2 Identify Command

The Identify Command returns the data described below.

Table 115 Identify Data Structure

Bytes	O/M	Default Value(Hex)	Description
01:00	M	1D97	PCI Vendor ID (VID)
03:02	M	1D97	PCI Subsystem Vendor ID
23:04	M	XXXXX	Serial Number
63:24	M	XXXXX	ModelNumber
71:64	M	VX.XX.XX	Firmware Revision
72	M	2h	Recommended Arbitration Burst
75:73	M	3a5a27h	IEEE OUI Identifier

Bytes	O/M	Default Value(Hex)	Description
76	O	0h	Controller Multi-Path I/O and Namespace Sharing Capabilities Bit 2: 1h - Controller is associated with an SR-IOV VirtualFunction 0h - Controller is associated with a PCI Function. Bit 1: 1h - Device has Two or More controller 0h - Device has One Controller Bit 0: 1h - Device has Two or More physical PCI Express ports 0h - Device has One PCI Express port
77	M	6h	Maximum Data Transfer Size
79:78	M	1h	ControllerID
83:80	M	10400h	Version
87:84	M	186a0h	RTD3ResumeLatency
91:88	M	7a120h	RTD3 Entry Latency
95:92	M	200h	Optional Asynchronous Events Supported
99:96	M	0h	Controller Attributes
101:100	O	0h	Read Recovery Levels Supported
110:102	-	0h	Reserved
111	M	1h	Controller Type
255:112	-	-	Reserved
257:256	M	17h	OptionalAdminCommand Support Bits 15:10 – Reserved Bit 9: 0h – Get Lba Status Not Supported Bit 8: 0h – Doorbell Config Not Suppported Bit 7: 0h – Virtualization Management Not Suppported Bit 6: 0h – Nvme Mi Send And Receive Not Supported Bit 5: 0h – Controler Directives Not Supported Bit 4: 1h – Device Self-Test Supported Bit 3: 0h - Namespace Management Attachment Not Supported Bit 2: 1h – Firmware Activate/Download Supported Bit 1: 1h - Format NVM Supported Bit 0: 1h Security Send and Security Receive Supported
258	M	2h	Abort Command Limit (Maximum number of concurrently outstanding Abort commands) (0's based value)
259	M	7h	Asynchronous Event Request Limit (Maximum number of concurrently outstanding Asynchronous Event Request commands) (0's based value)

Bytes	O/M	Default Value(Hex)	Description
260	M	16h	Firmware Updates Bits 7:5 - Reserved Bit 4 - 0h Support firmware activation without a reset Bits 3:1 - Number of firmware slots Bit 0 - 0h, "1" indicates Slot 1 is read-only
261	M	0h	Log Page Attributes Bits 7:5 – Reserved Bit 4: 0h - Not Support The Persistent Event log Bit 3: 1h - Support the Telemetry Host-Initiated and Telemetry Controller-Initiated log pages and sending Telemetry Log Notices Bit 2: 1h - Support extended data for the Get Log Page command Bit 1: 1h - Support the command effects log page Bit 0: 0h - Not support the SMART / Health Information log page on a per namespace basis
262	M	ffh	Error Log Page Entries (Number of Error Information log entries stored by controller) (0's based value)
263	M	4h	Number of Power States Support (0's based value)
264	M	1h	Admin Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates Admin Vendor Specific Commands use the format defined in NVM Express 1.0c Figure 8.
265	0	1h	Autonomous Power State Transition Attributes
267:266	M	167h	Warning Composite Temperature Threshold
269:268	M	16eh	Critical Composite Temperature Threshold
271:270	0	32h	Maximum Time for Firmware Activation
275:272	0	4000h	Host Memory Buffer Preferred Size
279:276	0	4000h	Host Memory Buffer Minimum Size
295:280	0	512GB:773C256000h 256GB: 3B9E656000h	Total NVM Capacity
311:296	0	0h	Unallocated NVM Capacity
315:312	0	0h	Replay Protected Memrory Block Support
317:316	0	fh	Extende Device Self-test Time
318	0	1h	Device Self-test Options
319	M	4h	Firmware Update Granularity
321:320	M	0h	Keep Alive Support
323:322	0	1h	Host Controlled Thermal Management Attributes (HCTMA)
325:324	0	111h	Minimum Thermal Management Temperature (MNTMT)

Bytes	O/M	Default Value(Hex)	Description
327:326	O	166h	Maximum Thermal Management Temperature (MXTMT)
331:328	O	0h	Sanitize Capabilities
335:332	O	0h	Host Memory Buffer Minimum Descriptor Entry Size
337:336	O	0h	Host Memory Maximum Descriptor Entries
511:338	-	-	Reserved
512	M	66h	Submission Queue Entry Size Bits 7:4 – 6h Max SQES (64 bytes) Bits 3:0 – 6h Required SQES (64 bytes)
513	M	44h	Completion Queue Entry Size Bits 7:4 – 4h Max CQES (16 bytes) Bits 3:0 – 4h Required CQES (16 bytes)
515:514	-	0h	Reserved
519:516	M	1h	Number of Namespaces
521:520	M	0h	Optional NVM Command Support Bits 15:8 – Reserved Bit 7 – 0h Not Support the Verify command Bit 6 – 1h Support Timestamp feature Bit 5 – 0h Support Reservations Bit 4 – 0h Not support Save field in Set Feature & Select field in Get Feature Bit 3 – 1h Write Zeros Supported 0h Not support Write Zeros Bit 2 – 1h Dataset Management Supported 0h Not support Dataset Management Bit 1 – 0h Write Uncorrectable Supported 0h Not support Write Uncorrectable Bit 0 – 1h Compare Supported 0h Not support Compare
523:522	M	0h	Fused Operation Support Bits 15:1 – Reserved Bit 0 – 0h Compare/Write Fused Operation Not Supported
524	M	0h	Format NVM Attributes Bits 7:3 – Reserved Bit 2 – 1h Cryptographic Erase is supprted 0h Cryptographic Erase is not supprted Bit 1 – 0h Cryptographic erase and user data erase Per Namespace Bit 0 – 0h Format Per Namespace

Bytes	O/M	Default Value(Hex)	Description
525	M	7h	Volatile Write Cache Bits 7:3 are reserved. Bits 2:1 – 11b indicate Flush command behavior (refer to section 6.8) if the NSID value is set to FFFFFFFFh as follows: 00b – Support for NSID field set to FFFFFFFFh is not indicated. 01b – Reserved 10b – The Flush command does not support the NSID field set to FFFFFFFFh 11b – The Flush command supports the NSID field set to FFFFFFFFh Bit 0 -1h Volatile write cache is present 0h No Volatile Write Cache present
527:526	M	0h	Atomic Write Unit Normal (0's based value)
529:528	M	0h	Atomic Write Unit Power Fail (0's based value)
530	M	1h	NVM Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates NVM Vendor Specific Commands use the format defined in NVM Express
531	-	0h	Reserved
533:532	0	0h	Atomic Compare & Write Unit
535:534	-	0h	Reserved
539:536	0	0h	SGL Support
544:767	-	-	Reserved
1023:768	M	nqn.2022-09.com.siliconmotion:nvm-subsystem-sn-XXXXXX	NVM Subsystem NVMe Qualified Name (SUBNQN)
1791:1024	-	0h	Reserved
2047:1792	-	-	NVMe over Fabrics specification
Power State Descriptors			
2079:2048	M	Refer to Identify Power State Descriptor Data Structure	Power State 0 Descriptor
2111:2080	0	Refer to Identify Power State Descriptor Data Structure	Power State 1 Descriptor
2143:2112	0	Refer to Identify Power State Descriptor Data Structure	Power State 2 Descriptor
2175:2144	0	Refer to Identify Power State Descriptor Data Structure	Power State 3 Descriptor
2207:2176	0	Refer to Identify Power State Descriptor Data Structure	Power State 4 Descriptor
…	-	0h	(N/A)
3071:3040	0	0h	Power State 31 Descriptor (N/A)
Vendor Specific			
4095:3072	-	0h	Vendor Specific

Table 116 Identify Power State Descriptor Data Structure

Bytes	Description	Power State 0 Descriptor(Hex)	Power State 1 Descriptor(Hex)	Power State 2 Descriptor(Hex)	Power State 3 Descriptor(Hex)	Power State 4 Descriptor(Hex)
255:184	Reserved	--	--	--	--	--
124:120	RelativeWriteLatency	0h	1h	2h	3h	4h
119:117	Reserved	--	--	--	--	--
116:112	RelativeWrite Throughput	0h	1h	2h	3h	4h
111:109	Reserved	--	--	--	--	--
108:104	Relative Read Latency	0h	1h	2h	3h	4h
103:101	Reserved	--	--	--	--	--
100:96	Relative Read Throughput	0h	1h	2h	3h	4h
95:64	ExitLatency	0h	0h	0h	1388h	61A8h
63:32	EntryLatency	0h	0h	0h	1388h	1388h
31:26	Reserved	--	--	--	--	--
25	Non-OperationalState	0h	0h	0h	1h	1h
24	Max Power Scale	1h	1h	1h	1h	1h
23:16	Reserved	--	--	--	--	--
15:0	Maximum Power	AFC8h	5DC0h	1770h	FAh	28h
255:184	Reserved	--	--	--	--	--

Table117 IdentifyNamespaceDataStructure

Bytes	O/M	Default Value(Hex)		Description
7:0	M	512GB	3B9E12B0h	Namespace Size
		256GB	1DCF32B0h	
15:8	M	512GB	3B9E12B0h	Namespace Capacity
		256GB	1DCF32B0h	
23:16	M	512GB	3B9E12B0h	Namespace Utilization
		256GB	1DCF32B0h	
24	M	0h		Namespace Features Bits 7:1 Reserved Bit 0: 0h Thin provisioning not supported
25	M	0h		Number of LBA Formats
26	M	0h		Formatted LBA Size Bits 7:5 – Reserved Bit 4: Metadata interleaved or separate (based on LBA format) Bit 3:0 – Indicates LBA format

Bytes	O/M	Default Value(Hex)	Description
27	M	0h	Metadata Capabilities Bits 7:2 – Reserved Bit 1 – Supports Metadata as separate buffer Bit 0 – Supports Metadata as extended LBA
28	M	0h	End-to-end Data Protection Capabilities Bits 7:5 – Reserved Bit 4 – Supports protection information as last 8 bytes of Metadata Bit 3 – Supports protection information as first 8 bytes of metadata Bit 2 – Supports Type 3 protection information Bit 1 – Supports Type 2 protection information Bit 0 – Supports Type 1 protection information
29	M	0h	End-to-End Data Protection Type Settings Bits 7:4 – Reserved Bits 3:1 – Protection information transferred as first 8 bytes of metadata Bit 3 – 0: Protection information transferred as last 8 bytes of metadata Bit 2:0 – 000b: Protection information disabled Bits 2:0 – 0h: Protection information is not enabled Bits 2:0 – 1h: Protection type 1 enabled Bits 2:0 – 2h: Protection type 2 enabled Bits 2:0 – 3h: Protection type 3 enabled
30	0	0h	NamespaceMulti-pathI/OandNamespacesharing Capabilities (NMIC) Bits 7:1 - Reserved Bit 0 - 1: Accessible by two or more controllers Bit 0 - 0: Private namespace
31	0	0h	Reservation Capabilities (RESCAP) Bit 7: version_reg Bit 6: Namespace supports the Exclusive Access (All Registrants reservation type) Bit 5: Namespace supports the Write Exclusive (All Registrants reservation type) Bit 4: Namespace supports the Exclusive Access (Registrants only reservation type) Bit 3: Namespace supports the Write Exclusive (Registrants only reservation type) Bit 2: Namespace supports the Exclusive Access Reservation type Bit 1: Namespace supports the Write Exclusive Reservation type Bit 0: Namespace supports the Persist Through Power Loss capability
32	0	0h	Format Progress Indicator Bit 7: fpi_supported Bits 6:0 - percentage_remainingg

Bytes	O/M	Default Value(Hex)		Description
33	0	1h		Deallocate Logical Block Features Bits 7:5 Reserved Bit 4: deallocate_guard_type Bit 3: deallocate_bit_write_zero_support Bits 2:0 – 0h: The read behavior is not reported Bits 2:0 – 1h: A deallocated logical block returns all bytes cleared to 0h Bits 2:0 – 2h: A deallocated logical block returns all bytes set to FFh
35:34	0	0h		Namespace Atomic Write Unit Normal
37:36	0	0h		Namespace Atomic Write Unit Power Fail
39:38	0	0h		Namespzce Atomic Compare & Write Unit
41:40	0	0h		Namespace Atomic Boundary Size Normal
43:42	0	0h		Namespace Atomic Boundary Offset
45:44	0	0h		Namespace Atomic Boundary Size Power Fail
47:46	0	0h		Reserved
63:48		512GB	773C256000h	NVM Capacity
		256GB	3B9E656000h	
103:64		0h		Reserved
119:104		275A3Ah		Namespace Globally Unique Identifier (NGUID) #:Variables *NGUID specifies data in a big endian format.
127:120		275A3Ah		IEEE Extended Unique Identifier(EUI64) #:Variables *EUI64 specifies data in a big endian format.
131:128		refer to 'LBA Format 0 Data Structure'		LBA Format 0 Support
135:132		0h		LBA Format 1 Support
139:136		0h		LBA Format 2 Support
143:140		0h		LBA Format 3 Support
147:144		0h		LBA Format 4 Support
151:148		0h		LBA Format 5 Support
155:152		0h		LBA Format 6 Support
159:156		0h		LBA Format 7 Support
163:160		0h		LBA Format 8 Support
167:164		0h		LBA Format 9 Support
171:168		0h		LBA Format 10 Support
175:172		0h		LBA Format 11 Support
179:176		0h		LBA Format 12 Support
183:180		0h		LBA Format 13 Support
187:184		0h		LBA Format 14 Support
191:188		0h		LBA Format 15 Support
383:192		0h		Reserved
4095:188		0h		Vendor Specific

Table 118 LBA Format 0 Data Structure

Bits	Name	Default Value(Hex)	Description
31:26	-	0h	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	9h	LBA Data Size
15:0	MS	0h	Meta data Size

6.3 NVM Express I/O Command Set

Table 119 NVMe I/O Command

Opcode (Hex)	Command Name
00h	Flush
01h	Write
02h	Read
09h	Dataset Management

6.4 Log Page Identify Support

Table 120 Log Identifier

Log Identifier (Hex)	Description
01h	Error Information
02h	SMART / Health Information
03h	Firmware Slot Information

6.5 Feature Identifiers Support

Table 121 Feature Identifier

Feature Identifier (Hex)	Description
04h	Temperature Threshold
07h	Number of Queues
08h	Interrupt Coalescing
09h	Interrupt Vector Configuration
0Dh	Host Memory Buffer

6.6 Smart/Health Information

Table 122 SMART Information

Bytes	Description
0	Critical Warning
2:1	Composite Temperature
3	Available Spare
4	Available Spare Threshold
5	Percentage Used
31:6	Reserved
47:32	Data Units Read
63:48	Data Units Written
79:64	Host Read Commands
95:80	Host Write Commands
111:96	Controller Busy Time
127:112	Power Cycles
143:128	Power On Hours
159:144	Unsafe Shutdowns
175:160	Media and Data Integrity Errors
191:176	Number of Error Information Log Entries
195:192	Warning Composite Temperature Time
199:196	Critical Composite Temperature Time
201:200	Temperature Sensor 1
203:202	Temperature Sensor 2
205:204	Temperature Sensor 3
207:206	Temperature Sensor 4
209:208	Temperature Sensor 5
211:210	Temperature Sensor 6
213:212	Temperature Sensor 7
215:214	Temperature Sensor 8
219:216	Thermal Management Temperature 1 Transition Count
223:220	Thermal Management Temperature 2 Transition Count
227:224	Total Time For Thermal Management Temperature 1
231:228	Total Time For Thermal Management Temperature 2
511:232	Reserved